Custoner´s information	
Titel **Delta ASPC2 Revision D / ASPC2 Revision E2**	

The goal of the following short description is to describes the differences between the ASICs ASPC2 Revisions D and ASPC2 Revision E2. Therefore the differencies between the two Revision are represented. Furthermore it is recommended to load the detailed description from internet. The internet address is
http://www.ad.siemens.de:8080/virlib/html_76/doc/index.htm → PROFIBUS-Description free of charge

Differencies from the user´s view

- **Size of FIFO,**
- **power input,**
- **The timing in peripheral mode and**
- **Quick-Access Mode**

Only these items are explained in this description.

A.) ASPC2 Revision D

Size of FIFO:

The size of the FIFO is adjustable from 64 /128 Byte (Mode-Register 2: FIFO-128Byte-Mode).

Power input:

The power input is approx. 0,8 W.

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Peripheral Mode

No.	Parameter	Min.	Max.	Unit
86	XWR/XWRL ↑ to XRD ↓ Inactive Delay	$1T_{48} + 4$ $1T_{48}$ $5T_{48}$ [3] **$5T_{48}$** [4] $9T_{48}$ [5]		ns ns ns ns ns

3) Read from IRR/IR after Write at IRR/IAR
Read from IR after Write from IMR
4) Read from Status-Reg. after Write at Mode-Reg. 1 (except ‘LASREAD=1’)
5) Read from LAS after Write 'LASREAD=1' (Mode-Reg. 1)

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7.5.2.1 SYS-Bus-Interface, Master-Mode

No.	Parameter	Min.	Max.	Unit
1	Clock High Time	5,2*	15,6*	ns
2	Clock Low Time	5,2**	15,6**	ns
3	Clock Rise- Fall Time		5,2	ns
10	Address to XRD ↓ Setup Time	27		ns
11	DT/XR Low to XRD ↓ Setup Time	19		ns
12	XRD Active Width	(2 + 2n)T48 1)		ns
13	Address valid to Data valid		2(n-1)T48 + 83	ns
14	Data to XRD ↑ Setup Time (8/16Bit-Mode)	27		ns
15	Data to XRD ↑ Hold Time (8Bit-Mode)	3		ns
	Hold Time (16Bit-Mode)	3		ns
16	DT/XR High to XRD ↑ Hold Time	20		ns
17	Address to XRD ↑ Hold Time	2T48		ns
18	XRD/XWR/XWRL↓↑ to XCLK2 " Setup Time	1T48		ns
19	Address to XWR/XWRL ↓ Setup Time	27		ns
20	XWR/XWRL Active Width	(2 + 2n)T48 1)		ns
21	Data Valid to XWR/XWRL ↑ Setup Time	(2+2n)T48-26		ns
22	Data to XWR/XWRL ↑ Hold Time	2T48		ns
23	Address to XWR/XWRL ↑ Hold Time	2T48		ns
	Quick-Access-Mode:			
25	Address to XRD ↓ Setup Time	7		ns
26	DT/XR Low to XRD ↓ Setup Time	0		ns
27	XRD Active Width	(1 + 2n)T48 1)		ns
28	Address valid to Data valid		2(n-1)T48 + 48	ns
29	Data to XRD ↑ Setup Time (8/16Bit-Mode)	20		ns
30	DT/XR High to XRD ↑ Hold Time	0		ns
31	Address to XWR/XWRL ↓ Setup Time	7		ns
32	XWR/XWRL Active Width	(1 + 2n)T48 1)		ns
33	Data Valid to XWR/XWRL ↑ Setup Time	(1+2n)T48-17		ns
35	XRDY to Clk48 ↑ Setup Time	5		ns
36	XRDY to Clk48 ↑ Hold Time	5		ns
37	XRDY Active Width	2T48+10		ns
38	XRDY ↓ to XRD/XWR ↑ Delay (kein zus. Waitstate)	2T48 2)	4T48 2)	ns
39	XRDY ↓ to XRD/XWR ↑ Delay (ein zus. Waitstate)	4T48 2)	6T48 2)	ns
40	Read-/Write-Cycle-Time (Quick-Access=0)	8T48 3)		ns
41	XRD; XWR/XWRL Inactive Delay zwischen aufeinanderfolgenden Wort-Zugriffen (Quick-Access=0)	4T48		ns
42	Read-/Write-Cycle-Time (Quick-Access=1)	6T48 3)		ns
43	XRD; XWR/XWRL Inactive Delay zwischen aufeinanderfolgenden Wort-Zugriffen (Quick-Access=1)	3T48		ns
44	XRD; XWR/XWRL Inactive Delay zwischen den beiden aufeinanderfolgenden Zugriffen im 8Bit-Mode	3/4T48		ns

* treshold 3,5V
** treshold 1V

1) n = number of waitstates
2) internal waitstates expired
3) based on 1 internal waitstate

Tabel 7.5-2: Specification of the processorbus-interface in master-mode

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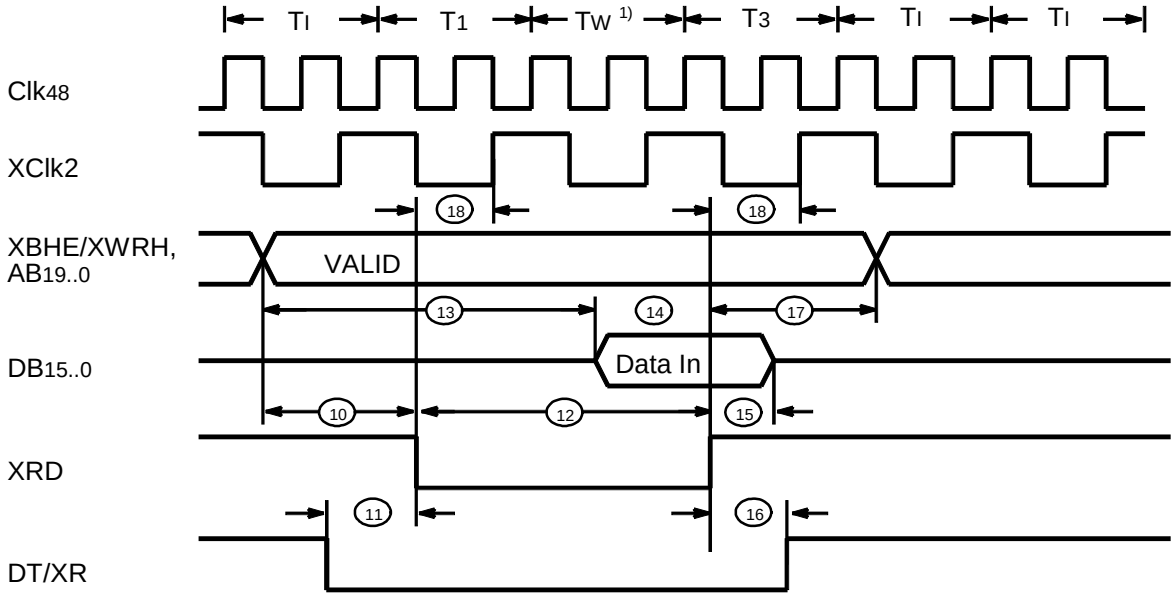
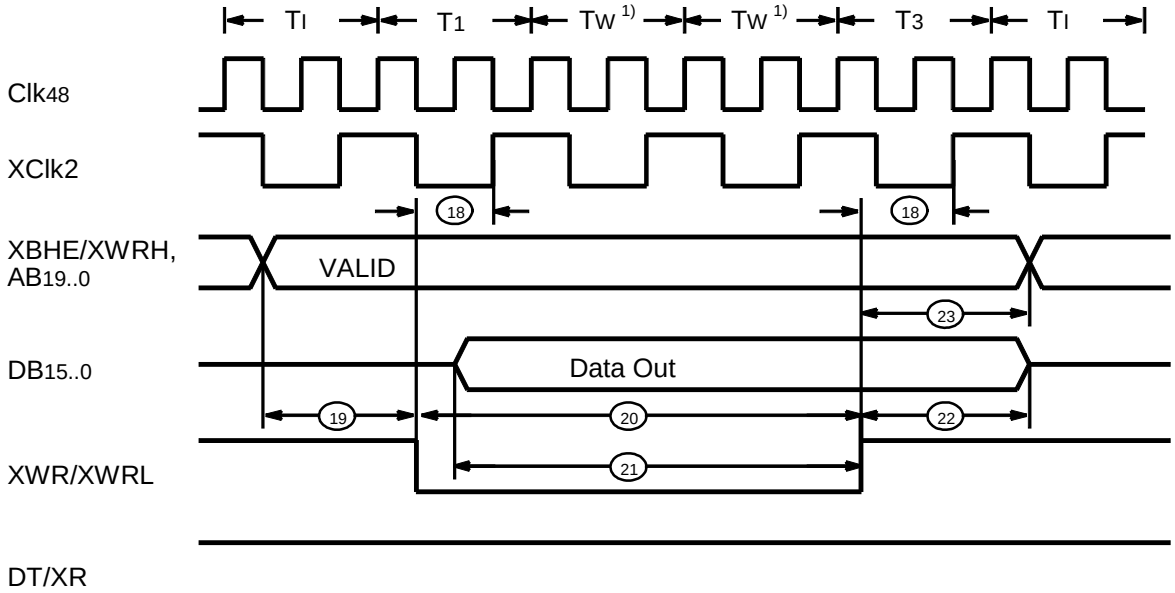


1) here 1 internal waitstate, ext. ready 'off'
2) XWR/XWRL = log.'1'

picture 7.5-4: Master-Mode (Quick-Access=0), ASPC 2 Read-Timing (without external ready)



1) here 2 int. waitstates, ext. Ready 'off
2) XRD = log.'1'

picture 7.5-5: Master-Mode (Quick-Access=0), ASPC 2 Write-Timing (without ext. Ready)

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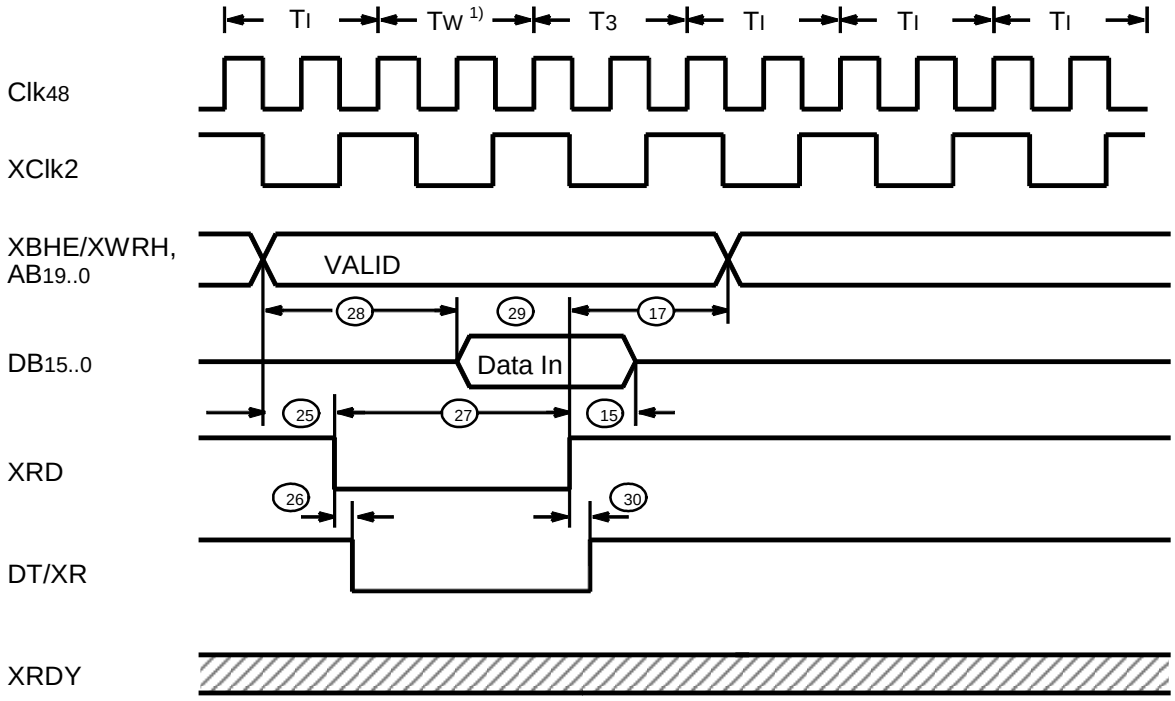
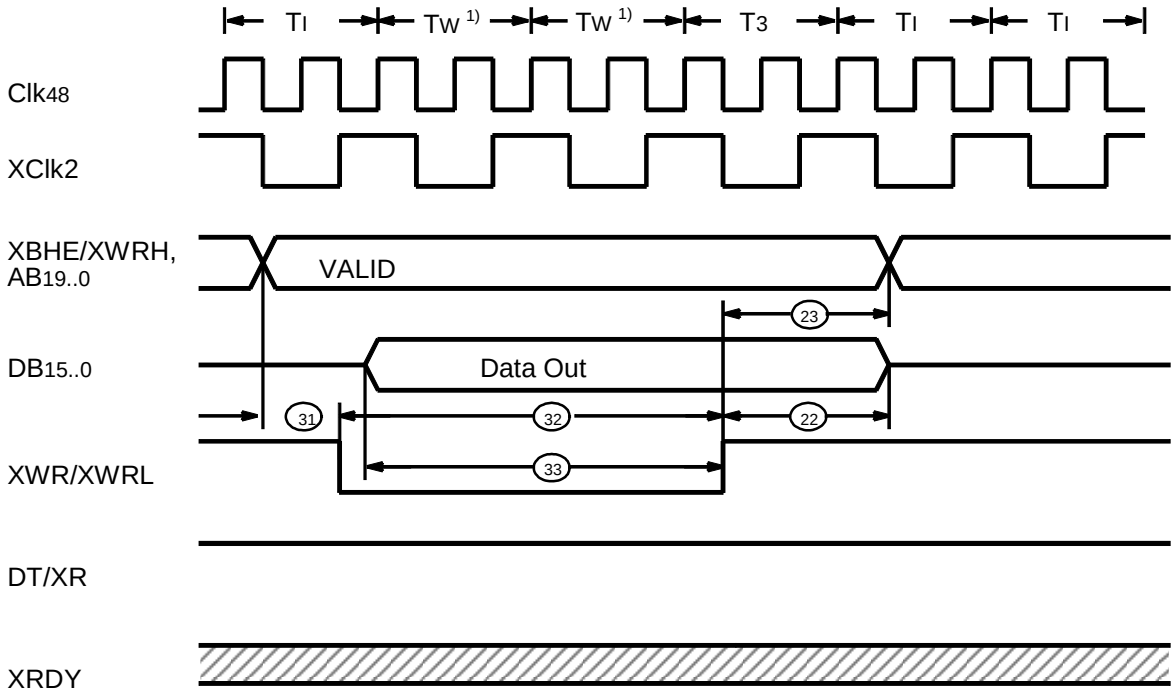


1) here 1 int. Waitstate, ext. Ready 'off'
2) XWR/XWRL = log.'1'

Picture 7.5-6: Master-Mode (Quick-Access=1), ASPC 2 Read-Timing (without ext. Ready)



1) here 2 int. Waitstates, ext. Ready 'off'
2) XRD = log.'1'

Picture 7.5-7: Master-Mode (Quick-Access=1), ASPC 2 Write-Timing (without ext. Ready)

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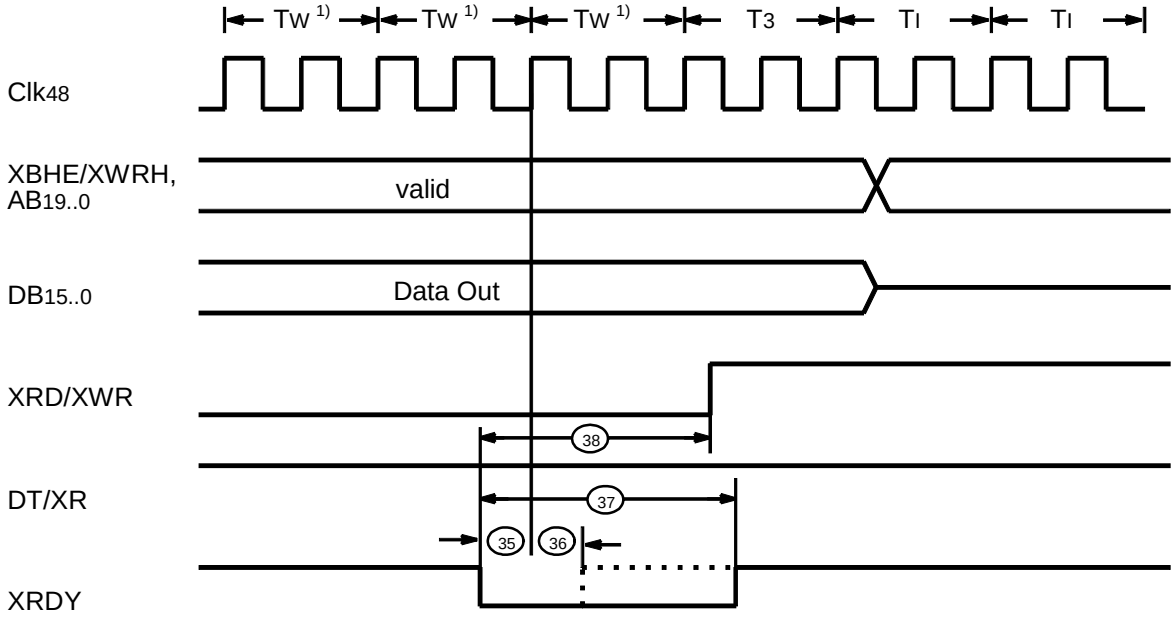
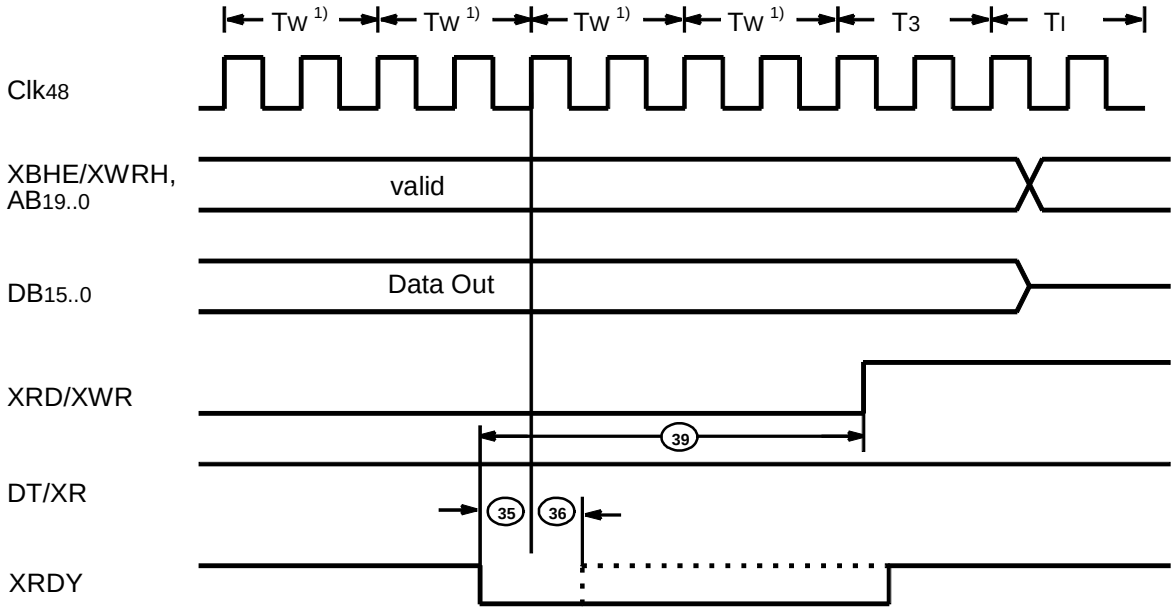


1) here int. Waitstate expired, ext. Ready 'on'

Picture 7.5-8: Master-Mode, ext. Ready-Timing (no additional waitstate after activating Ready)



1) here int. Waitstates expired, ext. Ready ein,
Additional waitstate after activating Ready

Picture 7.5-9: Master-Mode, ext. Ready-Timing (one additional waitstate after activating ready)

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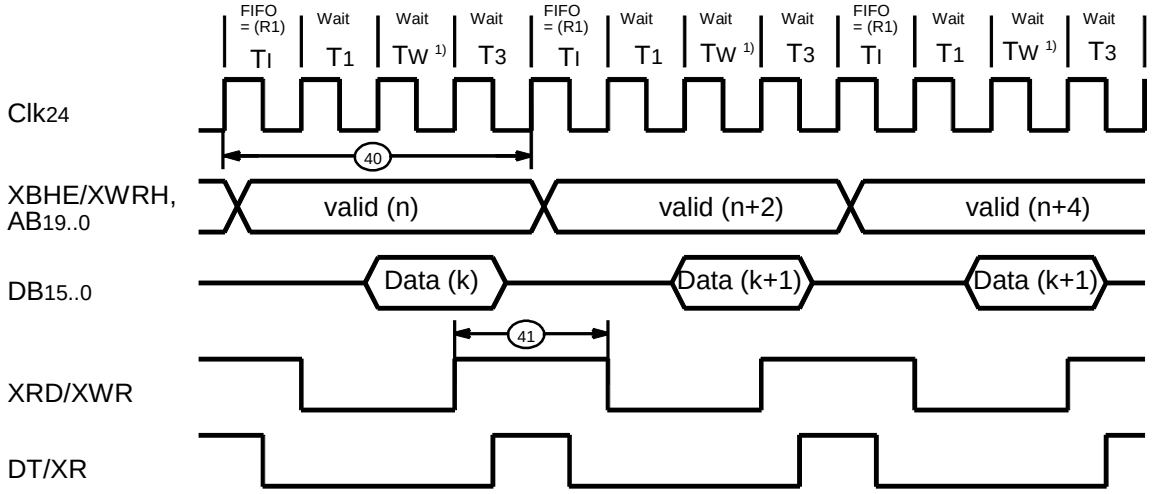
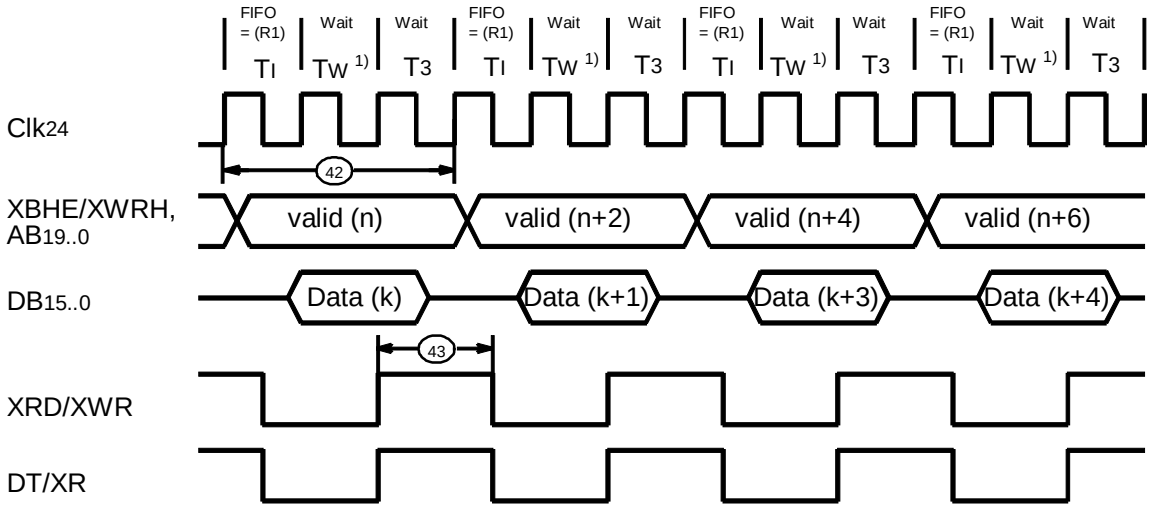


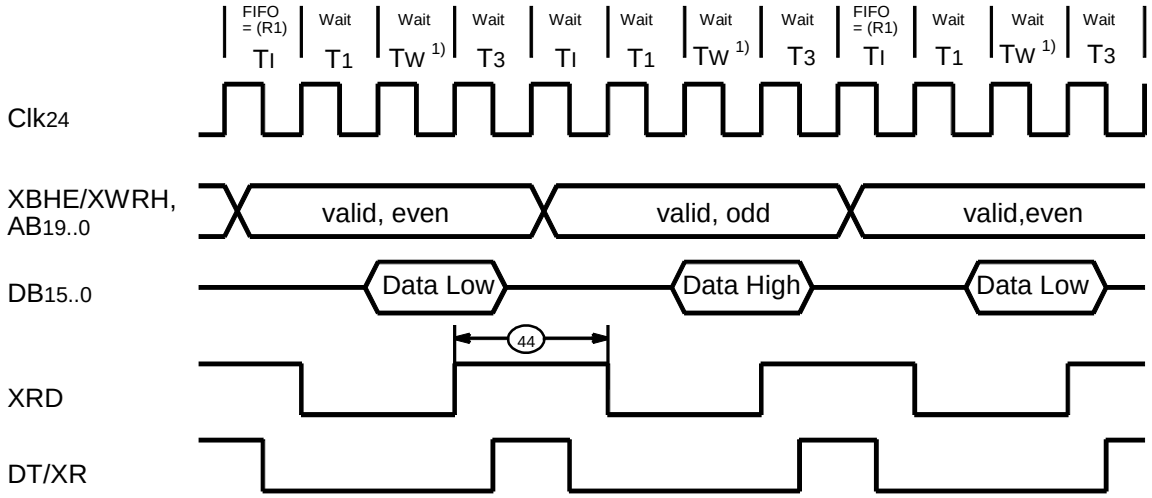
1) here 1 int. Waitstate, ext. Ready 'off

Picture 7.5-10: Master-Mode (Quick-Access=0), consecutive accesses to data-buffer)



1) hier 1 int. Waitstate, ext. Ready 'aus'

Picture 7.5-11: Master-Mode (Quick-Access=1), consecutive accesses to data buffer



1) here 1int. Waitstate, ext. Ready 'off'

Picture 7.5-12: Master-Mode (Quick-Access=0), 8Bit-Interface Read-Timing, Intel-Mode

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B) ASPC2 Revision E2

FIFO-size:
The size of the internal FIFO is adjustable fromf 64 up to 256 Bytes (Mode-Register 2: FIFO-256Byte-Mode).

Power input:
The power input is approx. 0,9 W.

Peripheral Mode

No.	Parameter	Min.	Max.	Unit
86	XWR/XWRL ↑ to XRD ↓ Inactive Delay	$1T_{48} + 4$ $1T_{48}$ $5T_{48}$ 3) **$6T_{48}$ 4)** $9T_{48}$ 5)		ns ns ns ns ns

3) Read from IRR/IR after Write to IRR/IAR
Read from IR after Write to IMR
4) Read from Status-Reg. after Write to Mode-Reg. 1 (except ‘LASREAD=1’)
5) Read from LAS after Write 'LASREAD=1' (Mode-Reg. 1)

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7.5.2.1 SYS-Bus-Interface, Master-Mode

No.	Parameter	Min.	Max.	Unit
1	Clock High Time	5,2*	15,6*	ns
2	Clock Low Time	5,2**	15,6**	ns
3	Clock Rise- Fall Time		5,2	ns
	Quick Access Mode=0:			
10	Address to XRD ↓ Setup Time	27		ns
11	DT/XR Low to XRD ↓ Setup Time	19		ns
12	XRD Active Width	$(2+2n)T_{48}$ 1)		ns
13	Address valid to Data valid		$2(n-1)T_{48} + 100$	ns
14	Data to XRD ↑ Setup Time (8/16Bit-Mode)	18		ns
15	Data to XRD ↑ Hold Time (8/16Bit-Mode)	3		ns
16	DT/XR High to XRD ↑ Hold Time	20		ns
17	Address to XRD ↑ Hold Time	$2T_{48}$		ns
18	XRD/XWR/XWRL ↓↑ XCLK2 ↑ Setup Time	0		ns
19	Address to XWR/XWRL ↓ Setup Time	27		ns
20	XWR/XWRL Active Width	$(2+2n)T_{48}$ 1)		ns
21	Data Valid to XWR/XWRL ↑ Setup Time	$(2+2n)T_{48} - 26$		ns
22	Data to XWR/XWRL ↑ Hold Time	$2T_{48}$		ns
23	Address to XWR/XWRL ↑ Hold Time	$2T_{48}$		ns
	Quick Access Mode=1:			
25	Address to XRD ↓ Setup Time	15		ns
26	DT/XR Low to XRD ↓ Setup Time	0		ns
27	XRD Active Width	$(1+2n)T_{48}$ 1)		ns
28	Address valid to Data valid		$2(n-1)T_{48} + 65$	ns
29	Data to XRD ↑ Setup Time (8/16Bit-Mode)	16		ns
30	DT/XR High to XRD ↑ Hold Time	0		ns
30a	Address to XRD ↑ Hold Time	1		ns
30b	Address to XWR ↑ Hold Time	1		ns
30c	Data to XWR ↑ Hold Time	1		ns
31	Address to XWR/XWRL ↓ Setup Time	13		ns
32	XWR/XWRL Active Width	$(1+2n)T_{48}$ 1)		ns
33	Data Valid to XWR/XWRL ↑ Setup Time	$(1+2n)T_{48} - 17$ 4)		ns
35	XRDY to Clk_{48} ↑ Setup Time	5		ns
36	XRDY to Clk_{48} ↑ Hold Time	5		ns
37	XRDY Active Width	$2T_{48} + 10$		ns
38	XRDY ↓ to XRD/XWR ↑ Delay (kein zus. Waitstate)	$2T_{48}$ 2)	$4T_{48}$ 2)	ns
39	XRDY ↓ to XRD/XWR ↑ Delay (ein zus. Waitstate)	$4T_{48}$ 2)	$6T_{48}$ 2)	ns
40	Read- / Write Cycle Time (Quick Access = 0)	$8T_{48}$ 3)		ns
41	XRD; XWR/XWRL Inactive Delay zwischen aufeinander-folgenden Wort-Zugriffen (Quick Access = 0)	$4T_{48}$		ns
42	Read- / Write Cycle Time (Quick Access = 1)	$4T_{48}$ 3)		ns
43	XRD; XWR/XWRL Inactive Delay zwischen aufeinander-folgenden Wort-Zugriffen (Quick Access = 1)	15		ns
44	XRD; XWR/XWRL Inactive Delay zwischen den beiden aufeinanderfolgenden Zugriffen im 8Bit-Mode	15		ns

* treshold 3,5V ** treshold 1V 1) n = number of Waitstates 2) internal Waitstates expired
3) 1based on internal waitstate

Tabel 7.5-2: Specifikation of the processorbus-interface, Master-Mode

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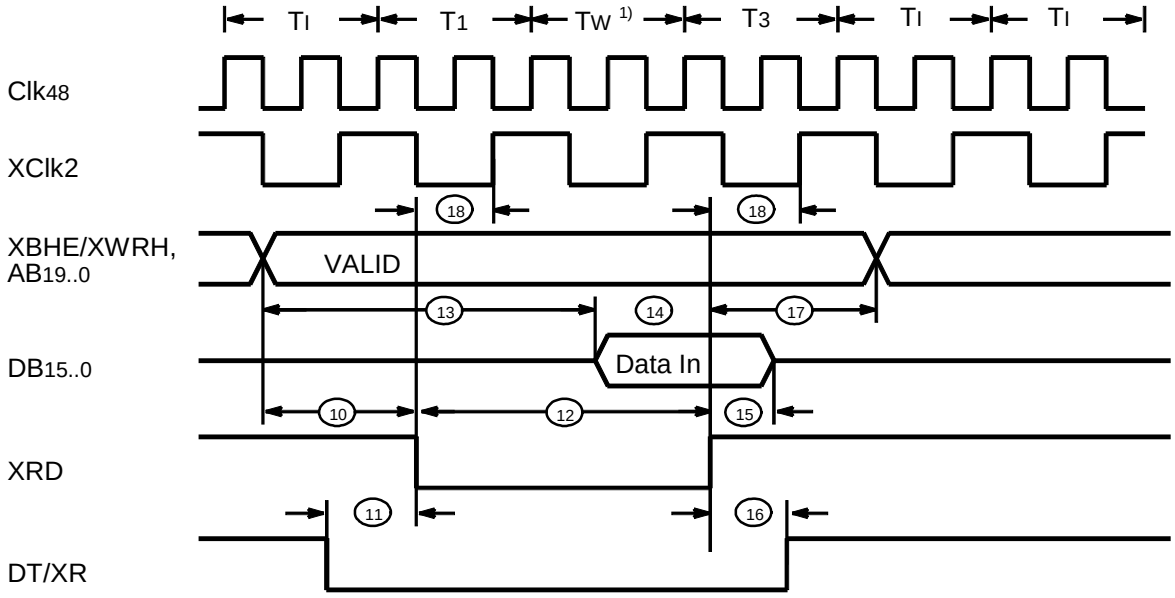
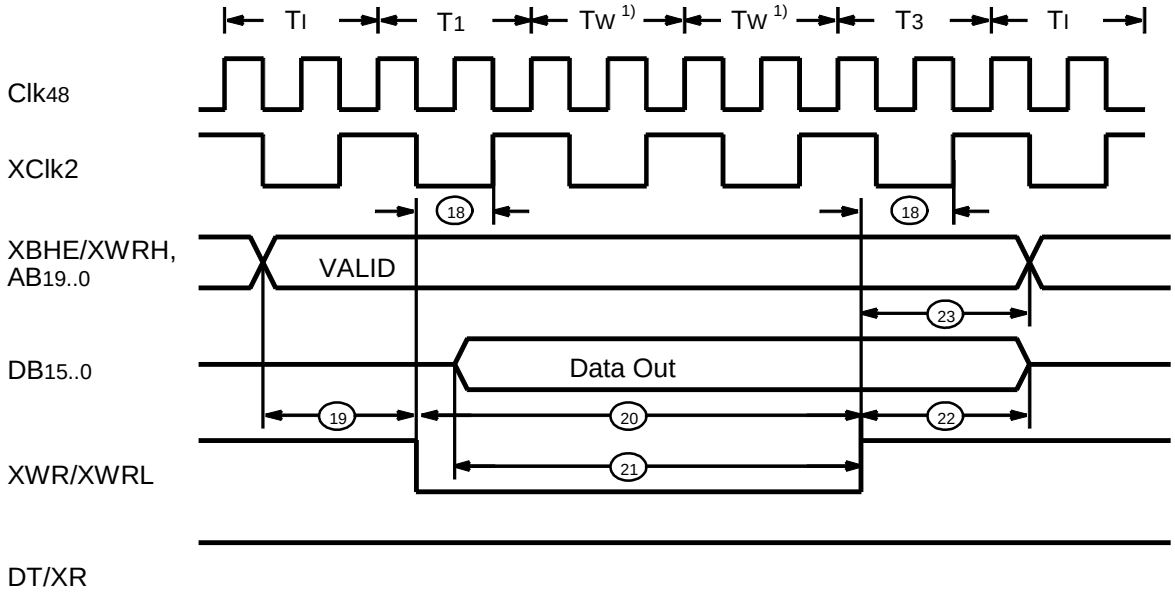


1) here 1 int. Waitstate, ext. Ready 'off'
2) XWR/XWRL = log.'1'

Picture 7.5-4: Master-Mode (Quick-Access=0), ASPC2 Read-Timing (without ext. Ready)



1) here 2 int. Waitstates, ext. Ready 'off'
2) XRD = log.'1'

Picture 7.5-5: Master-Mode (Quick-Access=0), ASPC2 Write-Timing (without ext. Ready)

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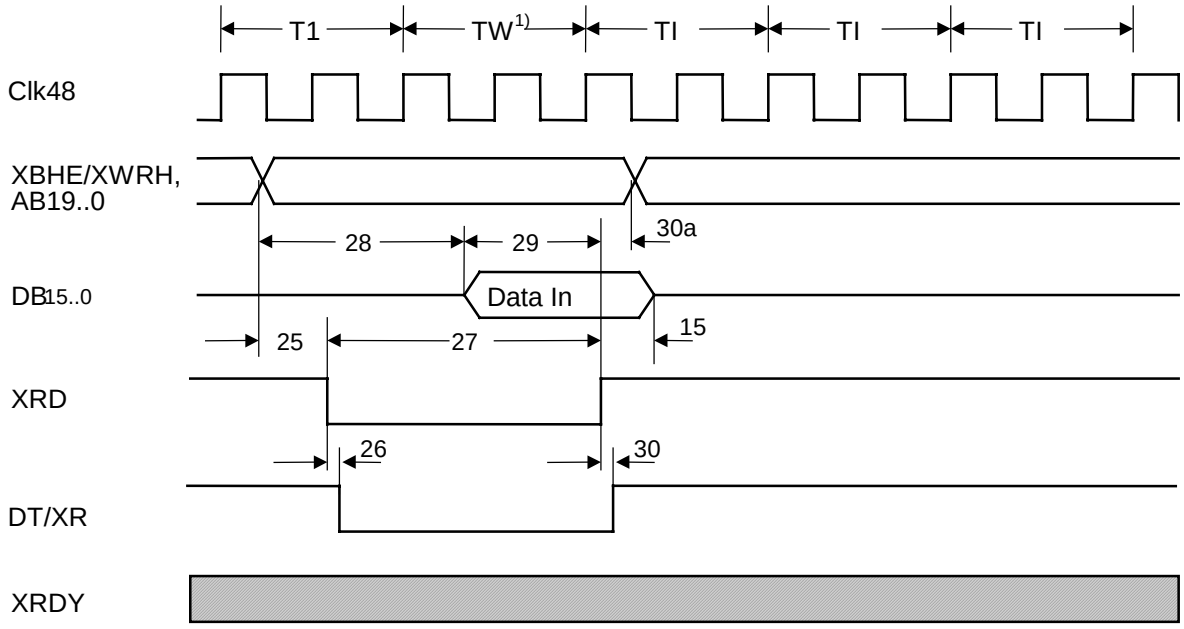
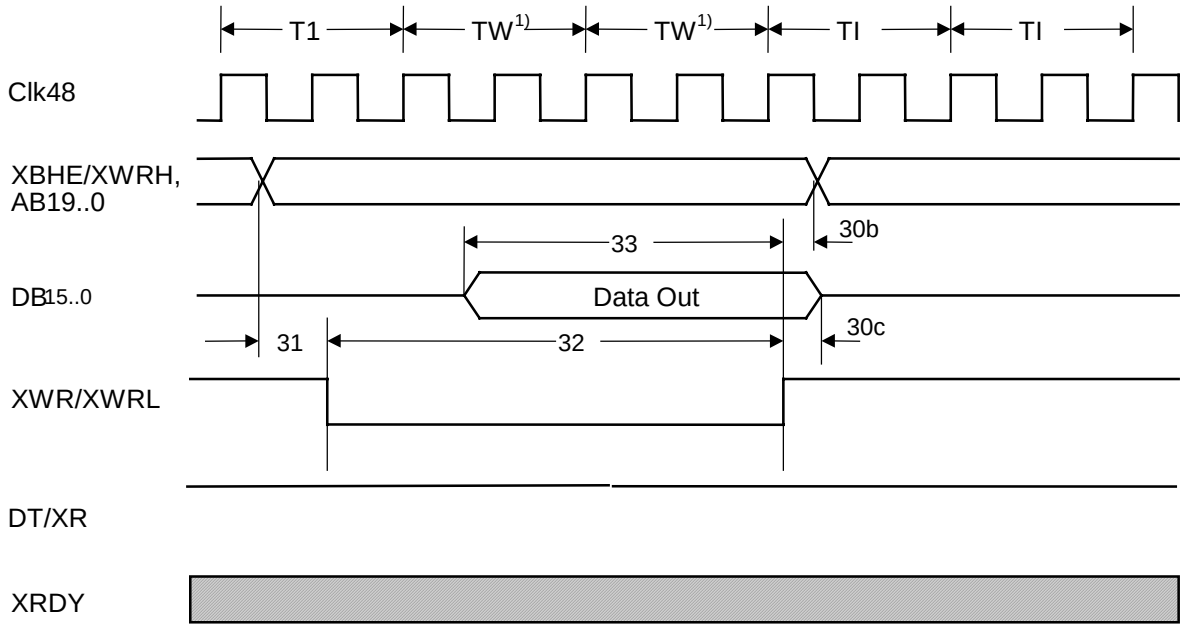


1) here 1 int. Waitstate, ext. Ready 'off'
2) XWR/XWRL = log.'1'

Picture 7.5-6: Master-Mode (Quick-Access=1), ASPC2 Read-Timing (without ext. Ready)



1) here 2 int. Waitstate, ext. Ready 'off'
2) XRD = log.'1'

Picture 7.5-7: Master-Mode (Quick-Access=1), ASPC2 Write-Timing (without ext. Ready)

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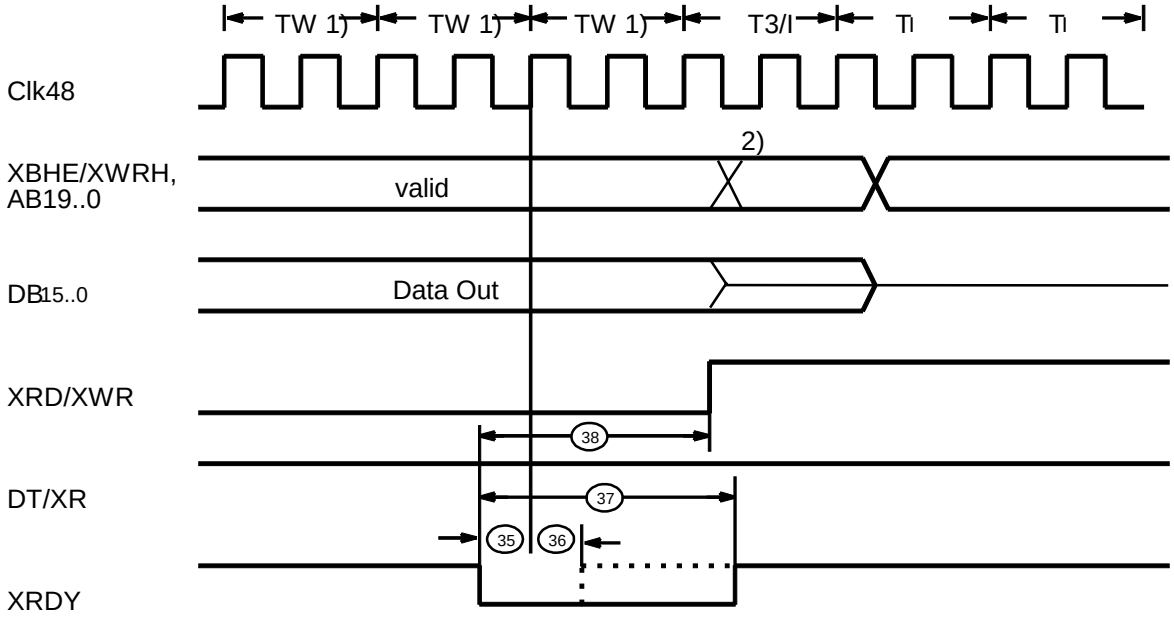
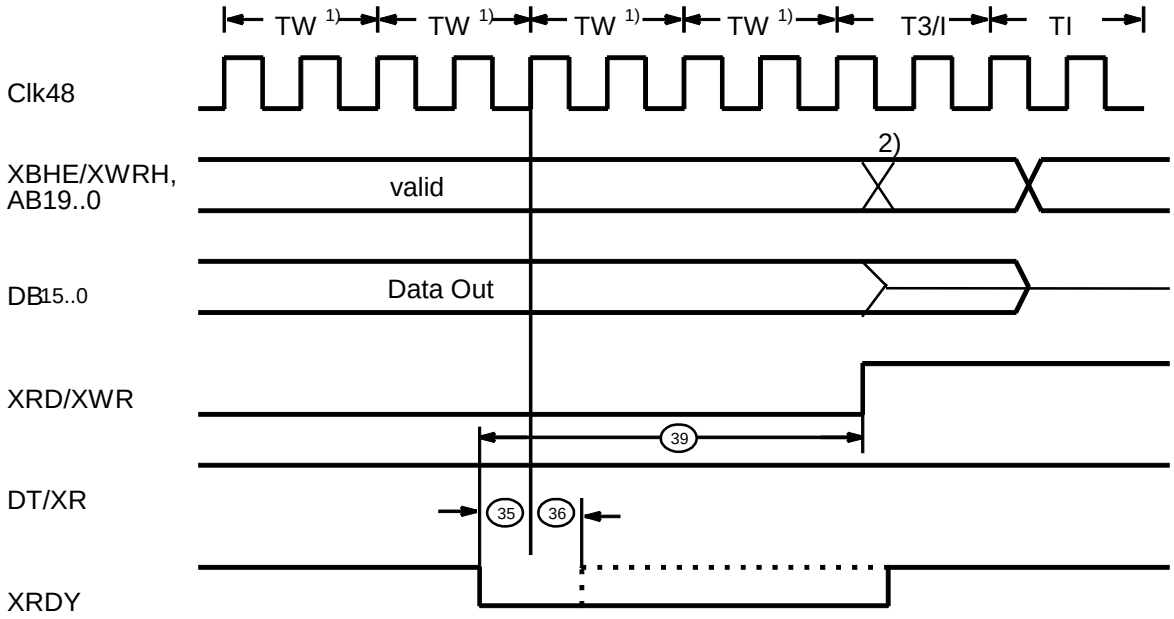


1) here int. Waitstates expired, ext. Ready 'on'
2) valid for Quick-Access=1

Picture 7.5-8: Master-Mode, ext. Ready-Timing (no additional waitstate after activating ready)



1) here internal waitstate expired, ext. Ready
Additional waitstate after activating ready

2) valid for Quick-Access=1

Picture 7.5-9: Master-Mode, ext. Ready-Timing (one additional waitstate after activating ready)

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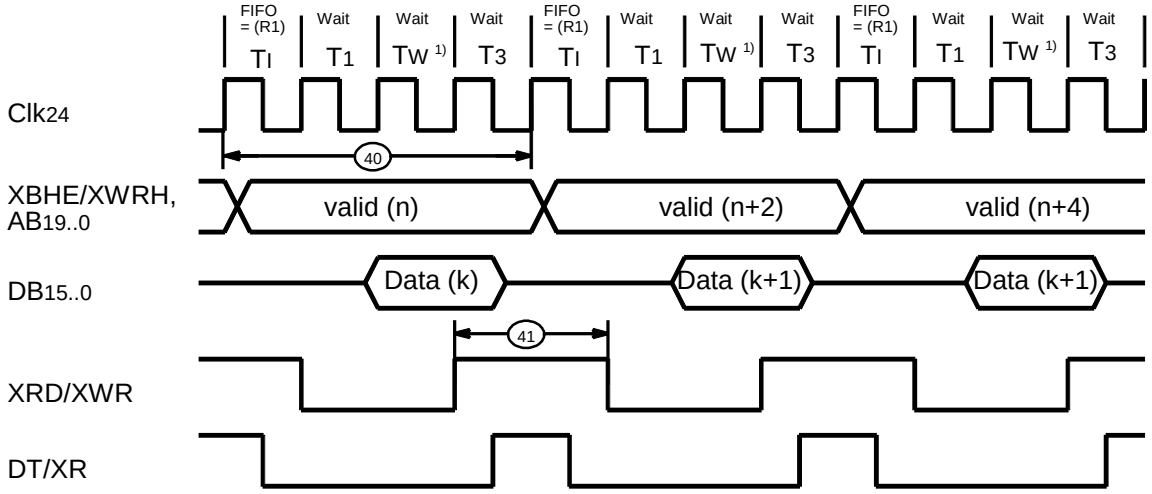
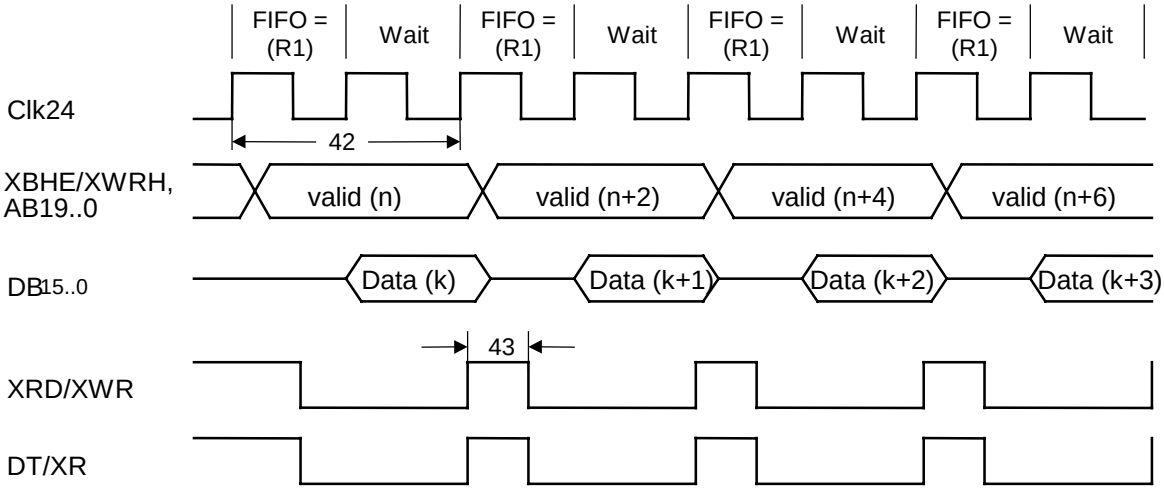


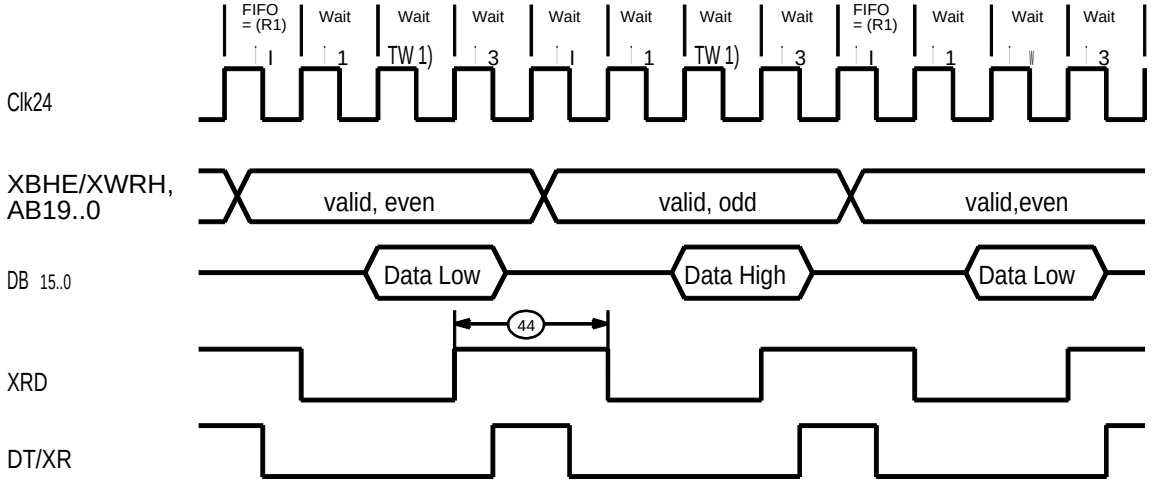
1) here 1 int. Waitstate, ext. Ready 'off'

Picture 7.5-10: Master-Mode (Quick-Access=0), consecutive accesses to data buffer)



1) here 1 int. Waitstates, ext. Ready 'off'

Picture 7.5-11: Master-Mode (Quick-Access=1), consecutive accesses to data buffer)



Picture 7.5-12: Master-Mode (Quick-Access=0), 8Bit-Interface Read-Timing, Intel-Mode

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