SIMATIC NET

LSPM2 Siemens PROFIBUS Multiplexer

User Description Date Dec 13th, 99

SIEMENS

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LSPM2

User Description

(Siemens PROFIBUS Multiplexer
according to EN 50 170)

Version: V1.7
Date: Dec 13th, 1999

Liability Exclusion
We have tested the contents of this document regarding agreement with the hardware and software described. Nevertheless, deviatations can't be excluded, and we are not guaranteeing complete agreement. The data in this document is checked periodically, however. Necessary corrections will be contained in subsequent versions. We gratefully accept suggestions for improvement.

Subject to technical changes.

Versions

Release	Date	Changes
V 1.7	Dec 13th, 1999	Chapter 3.1

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1 Introduction

Siemens offers its users some ASICs which support resp. fully handle data communication between the individual automation stations for simple and fast digital data exchange between programmable logic controllers.

The SPC (Siemens Profibus Controller) is based directly on Layer 1 of the OSI Model and requires an additional microprocessor for implementation of Layers 2 and 7. This permits all protocol types to be covered at the user end.

The SPC supports active and passive users on the bus system and filters off all external telegrams and errored wanted telegrams.

However, there are also simple devices, such as switches and thermocouples, in the field of automation which do not require a microprocessor for detection of their states.

A further ASIC with the designation LSPM2 (Lean Siemens Profibus Multiplexer) is available for low-cost adaptation of these devices. The LSPM2 operates as a Slave in the bus system. A Master addresses the LSPM2 via Layer 2 of the 7-Layer Model. After the LSPM2 has received an error-free telegram, it automatically generates the requested response telegrams (in accordance with DIN E 19245, Part 3).

2 Overview of functions

The LSPM2 has input/output ports which can be adapted directly to the periphery for data exchange with the periphery. The function blocks which the LSPM2 contains include the following:

The UART converts the parallel data of the I/O ports to a serial data stream for the L2 bus and vice versa.

The BAUD RATE GENERATOR generates baud rates of 9.6 kBd to 12 MBd. The clock for the baud rate generator can be supplied either by an external, connected crystal oscillator or by an external clock pulse generator.
Two operating modes are possible: -48 MHz clock and baud rates of 9.6 kBd to 12 MBd
-24 MHz clock and baud rates of 9.6 kBd to 6 MBd

The IDLE timer generates the bus idle time which is required for synchronising the listening users.

The integrated watchdog timer monitors the users present for addressability. In the event of an error, all ports are set to logical “0” in order to avoid malfunctions.

The I/O interface contains four input/output ports and one diagnostic port. The ports each have a width of eight bits. Two input/output ports can be configured as additional diagnostic ports by selecting a special operating mode.

The micro-sequencer (MS) performs the task of handling telegram communication and evaluating the individual functions, including automatic baud rate detection.

The USER interface state machine generates control signals for the MS and generates the status indication which the Master can request for evaluation.

The Profibus DP-specific parameters (station address and ID number) may be stored in external EEPROM or in a serial shift register. The interface configuration (input or output) is set via five pins on the LSPM2. An integrated control logic generates the signals for controlling the serial EEPROM or external shift register independently, depending on the external wiring used.

3 Pin description

The LSPM2 has an 80-pin QFP package (QFP80-P-1420B, Plastic Rectangular Flat Package) with the following signal pins:

PIN	Signal name	I/O	Function
1	XCTS	I	ClearToSend; PROFIBUS interface: The LSPM2 is Clear To Send if the XCTS signal is active
2	RXD	I	ReadData; PROFIBUS interface: input/receive data for LSPM2
3	RTS	O	RequestToSend: The LSPM2 requests Clear to Send with RTS=´1´
4	TXD	O	TransmitData; PROFIBUS interface: Output or transmit data from LSPM2
5	VSS		
6	PA0	I/O	
7	PA1	I/O	Data port A; can be programmed with parameters as an input or output port, depending on the
8	PA2	I/O	setting at the type inputs 0..4 (see Configuration Table I/O interface)
9	PA3	I/O	
10	PA4	I/O	
11	PA5	I/O	
12	VSS		
13	PA6	I/O	
14	PA7	I/O	
15	VDD		
16	PB0	I/O	
17	PB1	I/O	
18	PB2	I/O	Data port B; can be programmed with parameters as an input or output port, depending on the
19	PB3	I/O	setting at the type inputs 0..4 (see Configuration Table I/O interface)
20	PB4	I/O	
21	PB5	I/O	
22	PB6	I/O	
23	PB7	I/O	
24	VSS		
25	VDD		
26	PE0	I	
27	PE1	I	Diagnostic port E; the LSPM2 receives diagnostic information of the programmable data ports
28	PE2	I	or user-specific diagnosis via this port
29	PE3	I	
30	PE4	I	
31	PE5	I	
32	VSS		
33	VDD		
34	PE6	I	
35	PE7	I	
36	VSS		
37	PC0	I/O	
38	PC1	I/O	
39	PC2	I/O	Data port C; can be programmed with parameters as input, output or diagnostic port, depending
40	PC3	I/O	on the setting at the type inputs 0..4 (see Configuration Table I/O interface)
41	PC4	I/O	
42	PC5	I/O	
43	PC6	I/O	
44	PC7	I/O	
45	VDD		

PIN	Signal name	I/O	Function
46	PD0	I/O	
47	PD1	I/O	Data port D; can be programmed with parameters as input, output or diagnostic port, depending
48	PD2	I/O	on the setting at the type inputs 0...4 (see Configuration Table I/O interface)
49	PD3	I/O	
50	PD4	I/O	
51	PD5	I/O	
52	VSS		
53	PD6	I/O	
54	PD7	I/O	
55	VDD		
56	XRESET	I	Asynchronous Reset input; resets the LSPM2 to a defined initial state
57	RWCONS	O	ReadWriteCONSistent; output ´Read or Write Consistent´; signal for “pre-announcing” a following write or read access operation on the data ports; (see the Annex for signal timing)
58	XTEMO	I	Apply log<1> permanently to test pin (normal mode)
59	XTRI	I	Apply log<1> permanently to test pin (normal mode)
60	XSREE	I	Defines whether an external EEPROM or an external shift register (parallel in, ser.out) is connected to the LSPM2; log<1> ext. EEPROM, log<0>ext. shift register
61	FQ48	I	Operating frequency select pin log<1> 48 MHz; log<0> 24 MHz
62	DIAERROR	O	DIAgnosisERROR; this output is set when external diagnosis occurs
63	NORMOPER	O	NORMalOPERation; operating state indicator log<1> if parameter assignment telegram has been received with DA=TS (not in the case of broadcast tel.) log<0> after RESET and after each timeout of the WD timers
64	VSS		
65	TYP0	I	Type setting; the data ports (A-D) of the LSPM2 are programmed with these 5 pins;
66	TYP1	I	number of ports used, use as input or output ports, with/without consistency,
67	TYP2	I	extended diagnosis
68	TYP3	I	(see Configuration Table I/O interface)
69	TYP4	I	
70	VSS		
71	XTAL2	O	Oscillator output (see Wiring example)
72	XTAL1	I	Oscillator input (see Wiring example)
73	VDD		
74	VSS		
75	ACA	I	AddressChangeAllowed; with ACA signal active, it is possible, with the corresponding call telegram, to overwrite the EEPROM contents even with No_Add_Chg bit.
76	INTERCLK	O	INTERfaceCLocK; depending on pin XSREE, the LSPM2 generates clock sequences for the external EEPROM or external shift register via this signal.
77	INTERCS	O	INTERfaceChipSelect; depending on pin XSREE, the LSPM2 selects the external EEPROM or external shift register via this signal.
78	INTERDI	I	INTERfaceDataInput; LSPM2 receives input data from the external EEPROM or external shift register, depending on pin XSREE, via this channel.
79	INTERDOD	O	INTERfaceDataOutloaD; depending on pin XSREE, this output serves as a data channel to the EEPROM or as a data accept signal (parallel load) for loading data into the external shift register.
80	VDD		

Important:
The Pins for Type settings are only allowed to be changed when the ASIC is without voltage. Dynamical change of the Type settings while working is not permitted.
When switching on the power (voltage rise) the output RTS of the ASIC may be set. This is to be compensated by external wiring. See RESET wiring.

3.1 XTAL1, XTAL2 crystal oscillator connection

The LSPM2 has an internal oscillator with external crystal connection. Two different crystal frequencies are possible (24 MHz and 48 MHz). The 24 MHz version allows a 24 MHz external crystal connection or a 48 MHz harmonic-mode crystal to be connected. Various baud rates are available depending on the crystal used (wiring example, see below).

24 MHz -- 9.6 kBd to 6 MBd (external crystal connection or rystal oscillator)
48 MHz -- 9.6 kBd to 12 MBd (crystal oscillator)

In the 48 MHz version the LSPM2 must be operated with an external clock (e.g. crystal oscillator). In this case, the clock must be connected to the XTAL1 input, and the oscillator output XTAL2 must remain disconnected.

3.2 FQ48

This input informs the LSPM2 of what operating frequency is applied to pins XTAL1/2.

log.<0> 24 MHz
log. <1> 48 MHz

The input must be wired.

3.3 RWCONS

This output signal serves to pre-announce a consistent write or read access operation on the data ports.

Timing for this is described in Chapter 7.4.

3.4 ACA (AddressChangeAllowed)

With ACA signal active, it is possible, with a corresponding call telegram, to overwrite the EEPROM contents even with No_Add_Chg bit set (see Telegram structure, Chapter 5.).

log. <1> active TS address can be overwritten in the EEPROM

If the LSPM2 is operated with a shift register, this input does not function.

A defined level must be applied to the pin.

Attention: After Power on you can always overwrite the adress.

3.5 XSREE

This input defines whether the LSPM2 is operated with an external EEPROM or external shift register.

log. <0> ext. shift register
log. <1> ext. EEPROM

The input must be wired.

3.6 DIAERROR

This output serves to signal a diagnostic error and can be used to activate an LED. The output driver power is 4 mA.

log.<0>	no diagnostic error
log.<1>	diagnostic error, i.e. a log.<0> is applied to one of the diagnostic ports

Note: See Chapter 4.5 for further information on diagnosis.

3.7 NORMOPER

This output indicates the operating state of the LSPM2 on the Profibus L2 and can be used to activate an LED. The output driver power is 4 mA.

log.<0>	after Reset and each time after timeout of the watchdog timer
log.<1>	if a parameter assignment telegram destination address (DA) = station address (TS) has been received, i.e. if communication has been established with Master (Data-Exchange mode).

3.8 XTRI

Note: A defined level must be applied to all inputs.

VDD must be applied to the XTRI pin in normal mode.

3.9 XTEMO-Pin

Note: Defined levels must be applied to all inputs.

VDD must be applied to the XTEMO pin in normal mode.

4 Function description of the individual blocks

4.1 Watchdog timer

If malfunctions or disturbances occur on the bus line, it may be the case that the LSPM2 does not receive a telegram and, thus, the module's ports can no longer be operated. A WD is integrated in order to detect this situation. The WD timer is used initially for automatic baud rate detection after Reset.

When the correct baud rate has been detected, the MS switches the WD timer automatically to normal mode (Watchdog mode).

If WD mode is enabled, the timer is reset with each error-free telegram received, on recognition of the station number.

If a timeout of the timer occurs, i.e. no valid telegram detected, all outputs are reset ("0") and the system branches automatically to the automatic baud rate detection function.

The timeout time can be programmed in the COM-ET200. It is possible to select a value between 2 ms and 650 s, regardless of the set baud rate, thus permitting adaptation to the relevant system conditions.

The watchdog timeout times which can be set are calculated as follows:

T(WD) = factor * WD_1 * WD_2 Time factors 1 ms or 10 ms can be set via the parameter assignment telegram in the User_Prm_Data (see Telegram structure, Chapter 5.).

Setting WD_1=WD_2=1 is not permitted. In addition, neither WD_1 nor WD_2 may be 0!

4.2 Automatic baud rate detection

The LSPM2 is capable of detecting the baud rate automatically. The MS reverts automatically to the automatic baud rate detection function after each RESET and after WD timer timeout. No ports are manipulated during detection.

The MS always starts detection of the set baud rate with the highest baud rate and works through each baud rate sequentially until it has received any SD1 or SD2 telegram with no errors. This telegram may be routed to any user.

After detection of the correct baud rate, the MS reverts to normal mode (Watchdog mode).

Important: After false configuration or setting the bit UNLOCK in the parameter telegram, the LSPM2 returns to state WAIT_PRM, but doesn`t go to SEARCH BAUDRATE any more. This could make problems by changing the baudrate at the master at this moment.

Important: If the LSPM2 gets in state DATA_EXCHANGE a data telegram with more output bytes than selected at the ASIC, the LSPM2 answers with RS, but the ASIC remais in state DATA_EXCHANGE.

4.3 EEPROM interface (serial)

4.3.1 EEPROM parameters

The LSPM2 integrates a controller for a serial ext. EEPROM. Only one 16-bit word is ever stored as the parameter (EEPROM address 0H) or only two 16-bit words are ever read as the parameter (address 00H,01H).

Assignment EEPROM word 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								No_Add_Chg	TS address						
0	0	0	0	0	0	0	0		X	X	X	X	X	X	X

Assignment EEPROM word 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID number															
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

The ID number must be written to the EEPROM before connecting to the LSPM2 since only the TS address can be changed during write access via the LSPM2. Both data words are accessed only during read operations, i.e. an EEPROM programmed with the ID number must be used for production of a unit.

Attention: After Power on you can always overwrite the adress.

ID number:
The ID number serves as a unique identification of a DP Slave device type on the bus. An ID number is required for all DP Slave devices when reading diagnostic data, when writing parameter assignment data and when changing the station address via the bus. The ID number makes is possible for the DP Masters to identify the DP Slaves with minimal protocol effort.

An individual ID number is issued by the PNO (PROFIBUS User Organisation) for each device type. This ID number is not a serial number. Once a manufacturer has received an ID number for a device type from the PNO, he may use this number for each device of this type produced without having to ask for an ID number again each time from the PNO.

A separate ID number does not need to be applied for each revision level of devices which are basically identical but which differ as regards the number of inputs and outputs. The precondition is that the product can be described as a modular device in the GSD (device master file).

During the boot phase or after a RESET, the LSPM2 accepts the parameters (word 0, word 1) serially from an EEPROM and loads them into its internal parameter register.

The following values are permitted: TS address: 1.... 126D
ID number: all 16-bit values (as assigned by the PNO)

If the LSPM2 detects an illegal address (0 or 127D) when reading in, the MS automatically writes the default value TS=126D and No_Add_Chg=0 to the EEPROM. This permits parameter assignment of the station address with the corresponding tool (COM ET200).

4.3.2 EEPROM interface

The EEPROM control logic contained in the LSPM2 supports only serial modules with 5V supply, 16-bit organisation and integrated control logic. The control signals for EEPROMs with designation 93C46/47 are compatible EEPROMs (e.g. type OKI Datacode 16811 or higher) are generated. An ERASE/WRITE ENABLE cycle precedes each write cycle since the module is generally in DISABLE state after a power failure or power fade (i.e. it cannot be erased or written).

The LSPM2 internally triggers a write/read cycle with two flags (RD-EEPROM and WR-EEPROM), whereupon the EEPROM controller generates the corresponding control sequences for the output pins. When the cycle is completed, the controller acknowledges this by resetting the flags.

Signal name	I/O	Function	Status after RESET XSREE="1"
INTERCS	O	Chip-select for EEPROM	log. <0>
INTERCLK	O	Clock signal for EEPROM	log. <0>
INTERDI	I	DATA IN (Read EEPROM) (ST), READY after programming	-
INTERDOD	O	Data Out (Write EEPROM)	log. <0>

ST = Schmitt trigger

After the micro-sequencer (MS) has issued a read request to the controller, the read data is stored in a shift register and acknowledged by resetting the RD flag.

When writing the memory, the MS loads the data of the station address directly into the shift register of the EEPROM controller, provided the telegram has been received error-free by the LSPM2. During the write operation, the MS continues normal program processing. As soon as the memory chip has accepted the data, the controller acknowledges this by resetting the WD flag. If the LSPM2 receives a request to write the EEPROM, it acknowledges reception of the call telegram and then branches to the baud rate detection function.

A RESET during writing leads to undefined data in the EEPROM.

4.3.3 EEPROM control

Since the memory has a serial interface, the data, addresses and also the commands for switching over to the various operating modes must be transferred to it serially. The specified module awaits a 2-bit Op code after a start bit (log. "1") and then a 6-bit address, i.e. 9 bits, in order to switch to the corresponding mode. Data is read or written only after this.

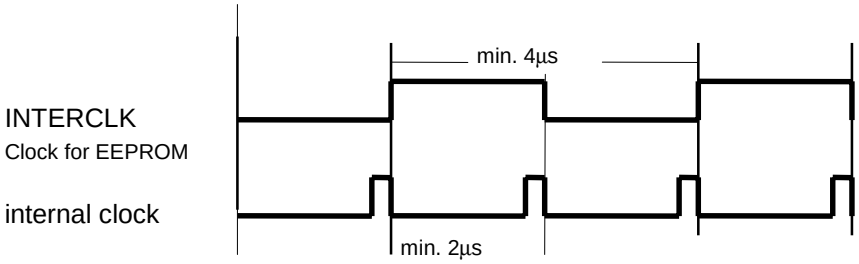
The following Op codes are generated:

Command	Start bit/Opcode	Address (binary)
READ WORD	110	000000 bzw. 000001
ERASE/WRITE-ENABLE	100	110000
WRITE WORD	101	000000

An erase cycle is not required since the memory overwrites the corresponding word when writing.

The word with address 000 000_{Bin} is generally addressed in the EEPROM, but an Erase/Write-Enable cycle is executed before each write access operation since the module is generally in Erase/Write-Disable mode after the power is restored.

The integrated controller of the LSPM2 generates a clock (INTERCLK) and a Chip-Select signal (INTERCS) with the corresponding timing and clocks the control bits and data out sequentially when writing or into an internal shift register when reading.



A read access operation takes 200 µs for one complete read cycle. A write cycle requires 100 µs, in addition to the programming time of approx. 10 ms per word.

Note: See Chapter 8 for a circuit example of connection of an EEPROM.

4.4 Shift register interface

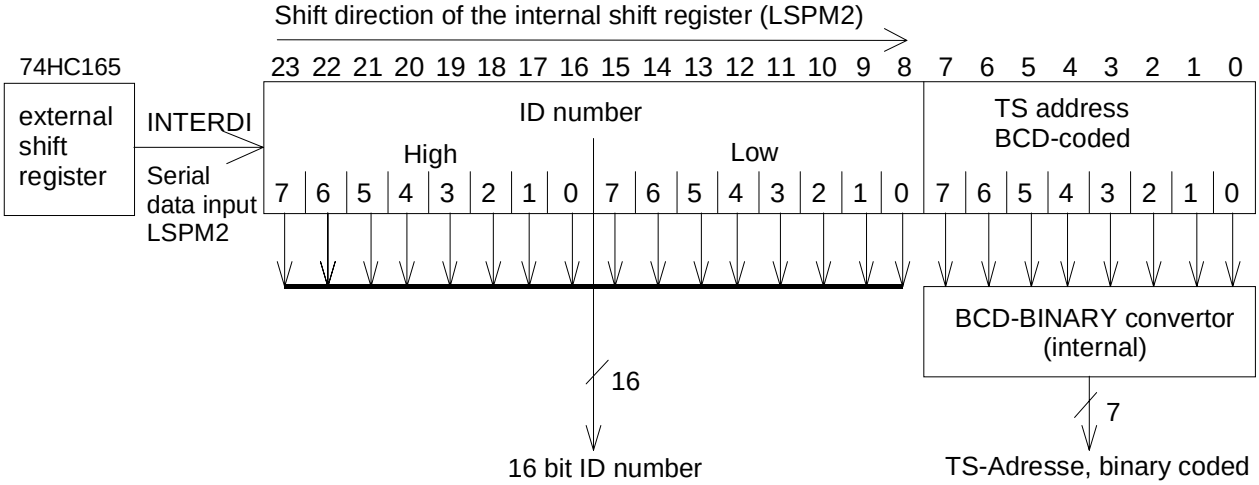
Besides the option of connecting an external EEPROM, the LSPM2 can also be wired with an external shift register (XSREE=0). In this case, the integrated shift register controller independently generates control sequences for shift registers with designation 74HC165 or compatible shift registers.

4.4.1 Shift register parameters

The internal shift register of the LSPM2 is written serially via bit position 23. The data are shifted to the right depending on the number of clock pulses still pending, i.e. the contents of position 23 are stored in bit 22, and the contents of position 22 are stored in bit 21 etc.

The following data sequence must be observed in this case at the serial data input (INTERDI):

first bit 0 (TS address) then bit 1 TS , bit 2 TS, bit 3 .....bit 0 ID no, bit 1 ID no.,.....etc.



A total of 24 bits must be stored in the external shift register: 16 bits for the ID number and 8 bits for the TS address.

The TS address must be set BCD-coded externally (values permitted are 1Dec to 99Dec). If the LSPM2 detects the illegal value 0Dec, the TS address is assigned 126Dec.

The externally set address is converted BCD-BINARY in the LSPM2 in order to permit the Slave address (TS) to be compared with the binary-coded destination address (DA) of the call telegram.

4.4.2 Shift register interface

The shift register controller is a block which is independent of the rest of the module and which is triggered only by the micro-sequencer (MS). The MS triggers a read cycle with a ReadShift flag, whereupon the shift register controller generates the corresponding control sequences for the interface pins. When the read cycle is complete, the controller acknowledges this by resetting the ReadShift flag.

If an external shift register is connected, the sequencer issues a read request to the controller after a RESET in order to accept the data in its parameter register.

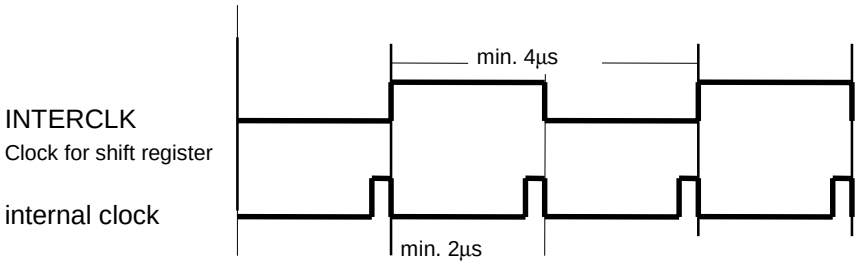
Signal name	I/O	Function	Status after RESET XSREE="0"
INTERCS	O	Clock Enable for shift register	log. <1>
INTERCLK	O	Clock signal for shift register	log. <0>
INTERDI	I	DATA IN (Read shift register), (ST)	-
INTERDOD	O	Accept signal for data to external shift register. (parallel load)	log. <1>

ST=Schmitt trigger

4.4.3 Control of the external shift register

The sequential control generates a clock (INTERCLK), a Clock Enable signal (INTERCS) and an Accept signal (INTERDOD) with the required timing and clocks the data sequentially into an LSPM2-internal shift register when reading.

When reading, the data is first loaded in parallel into the external shift register with the INTERDOD signal. From there, the data is clocked serially into the LSPM2-internal shift register (see Chapter Timing for timing).



The shift register controller operates with the same clock frequency as the EEPROM controller, i.e. 250 kHz. A read access operation takes 96 µs.

Note: See Chapter 8 for a circuit example.

4.5 I/O interface

The following ports are available to the user for detection and output of the various signals of a process sequence on site:

- two programmable 8-bit input/output ports (port A, port B
- two programmable 8-bit ports (port C, port D) which can be configured optionally as input/output ports or as additional diagnostic ports for recording errors.
- one 8-bit user-specific diagnostic port (port E

The various I/O configuration can be set via the parameter pins (type 0 to type 4), and the coding of the individual configuration is specified in the table below. In the case of “extended diagnosis”, bit-serial diagnosis for data ports A and/or D can be performed for instance via the diagnostic ports C and/or D. Port E is still available as an additional diagnostic port.

Attention: Please confirm that the Typ Pins are always set if Power off.

When using consistency the master documentations has to be attended!

Bei “erweiterter Diagnose” kann über die Diagnoseports C und/oder D z.B. bitweise Diagnose für die Datenports A und/oder B durchgeführt werden, Port E steht dabei weiterhin als zusätzlicher Diagnoseport zur Verfügung.

The ports not used (identified with a dash in the table) are programmed as outputs as standard and must not be wired on the PC board. The advantage of this over programming as inputs is that no pull-up resistors and no pads with internal pull resistors are required. (See Chapter Technical Data for the characteristic data of the input/output ports.)

Type assignment					Port configuration/consistency requirement					
<4>	<3>	<2>	<1>	<0>	Port A	Port B	Port C	Port D	Port E	Consist.
0	0	0	0	0	IN	-	-	-	Diagnosis	none
0	0	0	0	1	IN	IN	-	-	Diagnosis	none
0	0	0	1	0	IN	IN	IN	-	Diagnosis	none
0	0	0	1	1	IN	IN	IN	IN	Diagnosis	none
0	0	1	0	0	OUT	-	-	-	Diagnosis	none
0	0	1	0	1	OUT	IN	-	-	Diagnosis	none
0	0	1	1	0	OUT	IN	IN	-	Diagnosis	none
0	0	1	1	1	OUT	IN	IN	IN	Diagnosis	none
0	1	0	0	0	OUT	OUT	-	-	Diagnosis	none
0	1	0	0	1	OUT	OUT	IN		Diagnosis	none
0	1	0	1	0	OUT	OUT	IN	IN	Diagnosis	none
0	1	0	1	1	-	-	-	-	Diagnosis	none
0	1	1	0	0	OUT	OUT	OUT	-	Diagnosis	none
0	1	1	0	1	OUT	OUT	OUT	IN	Diagnosis	none
0	1	1	1	0	-	-	-	-	Diagnosis	none
0	1	1	1	1	OUT	OUT	OUT	OUT	Diagnosis	none
1	0	1	0	1	IN	IN	-	-	Diagnosis	overall
1	0	1	1	0	IN	IN	IN	IN	Diagnosis	overall
1	0	1	1	1	OUT	OUT	-	-	Diagnosis	overall
1	1	0	0	0	OUT	OUT	OUT	OUT	Diagnosis	overall
1	1	0	0	1	OUT	OUT	IN	IN	Diagnosis	overall
1	1	1	0	0	IN	IN	IN	-	Diagnosis	overall
1	1	1	0	1	OUT	OUT	OUT	-	Diagnosis	overall
1	1	1	1	0	OUT	OUT	OUT	IN	Diagnosis	overall
1	1	1	1	1	OUT	IN	IN	IN	Diagnosis	overall
extended diagnosis:										
1	0	0	0	0	IN	-	Diagnosis	-	Diagnosis	none
1	0	0	0	1	IN	IN	Diagnosis	Diagnosis	Diagnosis	none
1	0	0	1	0	OUT	-	Diagnosis	-	Diagnosis	none
1	0	0	1	1	OUT	OUT	Diagnosis	Diagnosis	Diagnosis	none
1	0	1	0	0	OUT	IN	Diagnosis	Diagnosis	Diagnosis	none
1	1	0	1	0	IN	IN	Diagnosis	Diagnosis	Diagnosis	overall
1	1	0	1	1	OUT	OUT	Diagnosis	Diagnosis	Diagnosis	overall

4.5.1 Structure of the diagnostic ports

The group diagnostic port (port E) is available to the user as a user-specific diagnostic port with 8 bits in any configuration. Two operating modes are basically possible for this port, and these operating modes can be set by the user with the parameter fag ENA_SAMMEL_DIA (see Telegram structure, Chapter 5.)

Flag=log.<0> log<0> at a pin of port E leads to a DIA_ERROR (DIAERROR output is set to log.<1>)

Flag=log.<1> Errors at pins E0 to E3 set the DIA_ERROR only if a channel diagnostic error is also pending at port C or port D.

An error at pins E4 to E7 always leads to a DIA_ERROR. (Regardless of ports C and D).

If programmed via the type pins, the LSPM2 also has two channel diagnostic ports (ports C and D) which it can use to monitor each of the I/O ports (ports A and B). If ports D and E are set as diagnostic ports, a log.<0> at one of the pins always leads to a DIA_ERROR which is forwarded in the LSPM2 internally as log.<1>.

The channel diagnostic ports can also be masked channel-by-channel (each bit) via mask registers. After a Reset, all masks are inactive. An error (log.<0>) at a channel diagnostic port is forwarded only if the corresponding mask bit is equal to zero (see also Chapter 5 Telegram structure SET_PARAM).

However, the user can also use all diagnostic ports for user-specific diagnosis. A log. <0> at a diagnostic input corresponds to a diagnostic error and sets the output pin DIA-ERROR on the LSPM2 to log. <1>. Output DIA-ERROR remains set until an error level is no longer applied to the diagnostic ports. The pin can be used to drive an LED. The driver power of the output is 4 mA.

In order to prevent unwired inputs of external diagnostic hardware leading permanently to a DIA_ERROR, the LSPM2 has an internal logic. This logic compares the current diagnostic data with the data last read in and generates an error only if a diagnostic change has occurred, i.e. each change is sent to the Master only once.

+5V must be applied via pull-up resistors to all unused inputs of the group diagnostic port and the programmed channel diagnostic port.

4.6 L2 interface

Transmission is performed in operating mode RS485 (RS485 physical).
Der LSPM2 hat hierfür folgende Pins:

Signal name	I/O	Type	Function
RTS	O	CMOS	Request to Send
TXD	O	CMOS	Transmit data
RXD	I	CMOS	Receive data
XCTS	O	CMOS	Clear to Send

Before sending, the LSPM2 sets the RTS signal to "1" and then loads the transmit buffer of the UART with the 1st character. The UART delays the first telegram character until signal CTS is active. $\overline{CTS}$ is no longer polled during telegram transmission. On completion of transmission (buffer empty stop bit is send), the RTS is reset. The XCTS pin must be set to log.<0> during operation.

Switching times:

No.	Symbol	Parameter	min.	Unit
1	TsRTS (TXD)	RTS ↑ to TXD (Setup-Time)	2	TBit*
2	ThRTS (TXD)	RTS ↓ to TXD (Hold-Time)	2	TBit*

*: 1 Tbit = 104µs at 9,6kBd, 1 TBit = 83ns at 12MBd

Timing:

Attention:
At Power on is it possible that the RTS signal is a short moment high. You must consider this in your application (see circuit diagramm).

The L2 interface is designed as in 9-pin SUB D connector with the following pin assignment:

Pin 1 - not used
Pin 2 - not used
Pin 3 - B line
Pin 4 - Request to Send (RTS)
Pin 5 - Ground 5V (M5)
Pin 6 - 5V potential (P5 floating approx. 100 mA)
Pin 7 - not used
Pin 8 - A line
Pin 9 - not used

The line screen must be connected to the housing.

Abschlußwiderstand in Busstecker / Busterminal (nach DIN19245):	ca. 10 mA
ET200 Handheld:	ca. 50 mA
optisches Busterminal SF/PF:	ca. 90 mA

Die Pinbelegung der freien Pins ist optional entsprechend DIN E 19245 Teil 3 zu verwenden.
The pin assignment of the free pins can be used optionally in accordance with DIN E 19245, Part 3.

Note: See Chapter 8 for a circuit example.

5 Telegram structure

The LSPM2 is a passive Slave user of PROFIBUS-DP. Required response telegrams are generated by the LSPM2 independently as soon as it has received a telegram destined for it free of errors from the Master. Telegram communication between Master and Slave has been kept simple and forms only a subset of the possible PROFIBUS telegrams.

In "normal mode" the LSPM2 processes only error-free SD1 or SD2 telegrams (StartDelimiter with value 10_{HEX} or 68_{HEX}) directed to it (correct TS address). Other telegrams are filtered. One exception is baud rate detection mode in which the LSPM2 can receive all telegrams (including SD3 and SD4 telegrams). However, it does not evaluate these telegrams but triggers only baud rate detection.

Only special features of the telegrams which it is essential to observe when using an LSPM2 Slave are described below.

5.1 Parameter telegram (SET_PARAM)

The Master transfers parameter assignment data to the LSPM2 with this telegram. 5 bytes USER parameter data must be transferred to the LSPM2 in addition to the 7 parameter bytes.

Byte	Bit position								Designation
	7	6	5	4	3	2	1	0	
6									
7	0	0	0	0	EN_ Sammel_ Dia	WD_ Base	0	0	User_Def_PRM1
8									Mask for Diaport1
9									Mask for Diaport2
10	0	0	0	0	0	0	0	0	User_Def_PRM2
11	0	0	0	0	0	0	0	0	User_Def_PRM3

Byte 0-6: Parameter assignment data, see DIN E 19425, Part 3

Byte 7: User_Def_PRM1

Bit 0,1: are reserved and must be set to 0

Bit 2: The WD base bit defines the timebase with which the watchdog is clocked
´0´= timebase 10 ms (status after Reset) ´1´= timebase 1 ms

Bit 3: This bit activates group diagnostic mode.

EN_Sammel_Dia = 0 A channel diagnostic error of port D and E is always signalled.
EN_Sammel_Dia = 1 An error at pins E0-E3 is signalled to the Master only if a channel diagnostic error also occurs.

Error changes at the channel diagnostic ports and pins E4-E7 of the group diagnostic port are, however, still forwarded immediately.

IMPORTANT: If a type configuration without channel diagnosis (port C and D) is set, EN_Sammel_Dia must be programmed as 0!

Bit 4-7: are reserved and must be set to 0

Byte 8, 9,: Mask bytes for diagnostic ports

Byte 8 contains the mask bits for diagnostic byte 1 (port C) and byte 9 contains the mask bits for diagnostic byte 2 (port D). The mask bits are assigned to the corresponding bit positions of the diagnostic ports. A ´1´ at the corresponding bit position masks diagnosis, i.e. these bits are masked. All masks are cleared after Reset.

IMPORTANT: If a type configuration without diagnosis is set, the mask bits must be programmed as 00_{HEX}!

Byte 10, 11: User_Def_PRM2/3

These bytes are currently not yet used for checking purposes and must be set to ´0´.

5.2 Diagnostic telegram (SLAVE_DIAG)

The LSPM2 sends diagnostic data to the Master with this telegram. A ´1´ at a bit position signifies that the corresponding event has occurred.

A further 7 bytes of external diagnostic data, described in the following table, are sent by the LSPM2, in addition to the 6 bytes diagnostic data. Diagnostic data is transferred only after a change of the pending data. One exception to this is Freeze mode.

IMPORTANT: If Freeze mode is activated, the diagnostic data is also frozen. A telegram is thus sent to the Master not with a change in diagnostic data but only after a further ´Freeze´.

Byte	Bit position								Designation
	7	6	5	4	3	2	1	0	
5									
6	0	0	0	0	0	1	1	1	Diag_Header
7	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	Port diagnosis (port E)
8	0	0	0	0	0	0	0	0	Diag_Reserved_1
9	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	Port C (only with extended diagnosis, otherwise 00_{HEX})
10	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	Port D (only with extended diagnosis, otherwise 00_{HEX})
11	0	0	0	0	0	0	0	0	Diag_Reserved_2
12	0	0	0	0	0	0	0	0	Diag_Reserved_3

Byte 6: Diag_Header

This byte contains the LSPM2-specific number of external diagnostic bytes, i.e. value 07_{HEX} is entered at this point on the LSPM2.

Byte 7: Group diagnosis

This byte contains the diagnostic data of the signals pending at port E. A diagnostic error at one of the pins (log.<0>) is forwarded inverted, i.e. the error is indicated with ´1´ at the corresponding bit position.

Byte 8, 11, 12: Diag_Reserved

These bytes are reserved. The LSPM2 always sends value 00_{HEX} at this point.

Byte 9, 10: channel diagnosis port C, port D

This byte contains the diagnostic data of the signals pending at port C and port D. A diagnostic error at one of the pins (log.<0>) is forwarded inverted, i.e. the error is indicated with ´1´ at the corresponding bit position. If no extended diagnosis is set via the type coding, value 00_{HEX} is always entered at this point.

5.3 Configuration telegram (GET_CONFIG)

The Master transfers the configuration data to the LSPM2 with this telegram. The LSPM2 always expects 2 code bytes. The following sequence must be observed.

Byte	Bit position								Designation
	7	6	5	4	3	2	1	0	
0	0/1	0	1	0	0	0	0/1	0/1	Code byte_Outputs
1	0/1	0	0	1	0	0	0/1	0/1	Code byte_Inputs

Byte 0: Code byte_Outputs

Following values permitted:

without consistency	Overall consistency
20_{Hex} with 1 output	$A0_{Hex}$ with 1 output
21_{Hex} with 2 outputs	$A1_{Hex}$ with 2 outputs
22_{Hex} with 3 outputs	$A2_{Hex}$ with 3 outputs
23_{Hex} with 4 outputs	$A3_{Hex}$ with 4 outputs
00_{Hex} with 0 outputs	00_{Hex} with 0 outputs

Byte 1: Code byte_Inputs

Following values permitted:

without consistency	Overall consistency
10_{Hex} with 1 input	90_{Hex} with 1 input
11_{Hex} with 2 inputs	91_{Hex} with 2 inputs
12_{Hex} with 3 inputs	92_{Hex} with 3 inputs
13_{Hex} with 4 inputs	93_{Hex} with 4 inputs
00_{Hex} with 0 inputs	00_{Hex} with 0 inputs

5.4 Optional services

The LSPM2 basically supports SYNC and FREEZE mode, i.e. if a SYNC or FREEZE is set in the Global_Contol_Service, this function is executed.

Note: If FREEZE mode is activated, the diagnostic data is also frozen. A change is not signalled to the Master until a further FREEZE is transmitted.

5.5 Other services

The LSPM2 supports services Set_Slave_Adress (if using a serial EEPROMs), Read_Inputs, Read_Outputs, Get_Config.

6 Technical data

Maximum limit values

Parameter	Desig.	Min	Max	Unit
Supply Voltage	V_{DD}	V_{SS*} - 0.3	7,0	V
Leakage Power	P_{max}		190	mW
Input Voltage	V_I	V_{SS*} - 0.3	V_{DD} + 0.3	V
Input Current	I_I	- 10	+ 10	mA
Storage Temperature	T_{stg}	- 40	+ 125	^oC
Junction Temperature	T_J		+ 125	^oC

* V_{SS} = 0V

Important: Long-term operation with these values reduces the module's service life.

Permitted operating ratings

Parameter	Desig.	Min	Type	Max	Unit
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input High Voltage	V_{IHC}	3.5	-	-	V
Input Low Voltage	V_{ILC}	-	-	1.5	V
Schmitt trigger:					
Input High Voltage	V_{IHC}	4	-	-	V
Input Low Voltage	V_{ILC}	-	-	1.0	V
Operating Temperature	T_{op}	- 40		+ 75	^oC

DC specification of the I/O driver

Parameter	Desig.	Condition	Min	Type	Max	Unit
Output High Voltage	V_{OH}	-	V_{DD} - 0.8			V
Output Low Voltage	V_{OL}	-			0,4	V
Input Leakage Current	I_{LI}	-	- 10		10	µA

Signal line	Driver type	Driver strength	max. cap. load
$PA_{7....0}$ to $PH_{7....0}$	Tristate	4 mA	50 pF
TXD	Tristate	8 mA	50 pF
RTS	Tristate	8 mA	50 pF
NORMOPER	Tristate	4 mA	50 pF
DIAERROR	Tristate	4 mA	50 pF
INTERCLK	Tristate	4 mA	50 pF
INTERCS	Tristate	4 mA	50 pF
INTERDOD	Tristate	4 mA	50 pF
RWCONS	Tristate	4 mA	50 pF
XTAL2	Buffer	4 mA	50 pF

Pins of the LSPM2

Inputs:	Qty.	I/O	Type
ACA	1	IN	Normal
FQ48	1	IN	Normal
PE7...0	8	IN	Schmitt trigger
INTERDI	1	IN	Schmitt trigger
RXD	1	IN	Schmitt trigger
XTEMO	1	IN	Normal
XTRI	1	IN	Normal
XSREE	1	IN	Normal
TYP4...0	5	IN	Normal
CTS	1	IN	Schmitt trigger
XRESET	1	IN	Schmitt trigger
XTAL1	1	IN	Clock buffer

Outputs:	Qty. I	I/O	Type
DIAERROR	1	OUT	4 mA buffer
INTERCLK	1	OUT	4 mA buffer
INTERCS	1	OUT	4 mA buffer
INTERDOD	1	OUT	4 mA buffer
NORMOPER	1	OUT	4 mA buffer
RWCONS	1	OUT	4 mA buffer
RTS	1	OUT	4 mA buffer
TXD	1	OUT	4 mA buffer
XTAL2	1	OUT	4 mA buffer

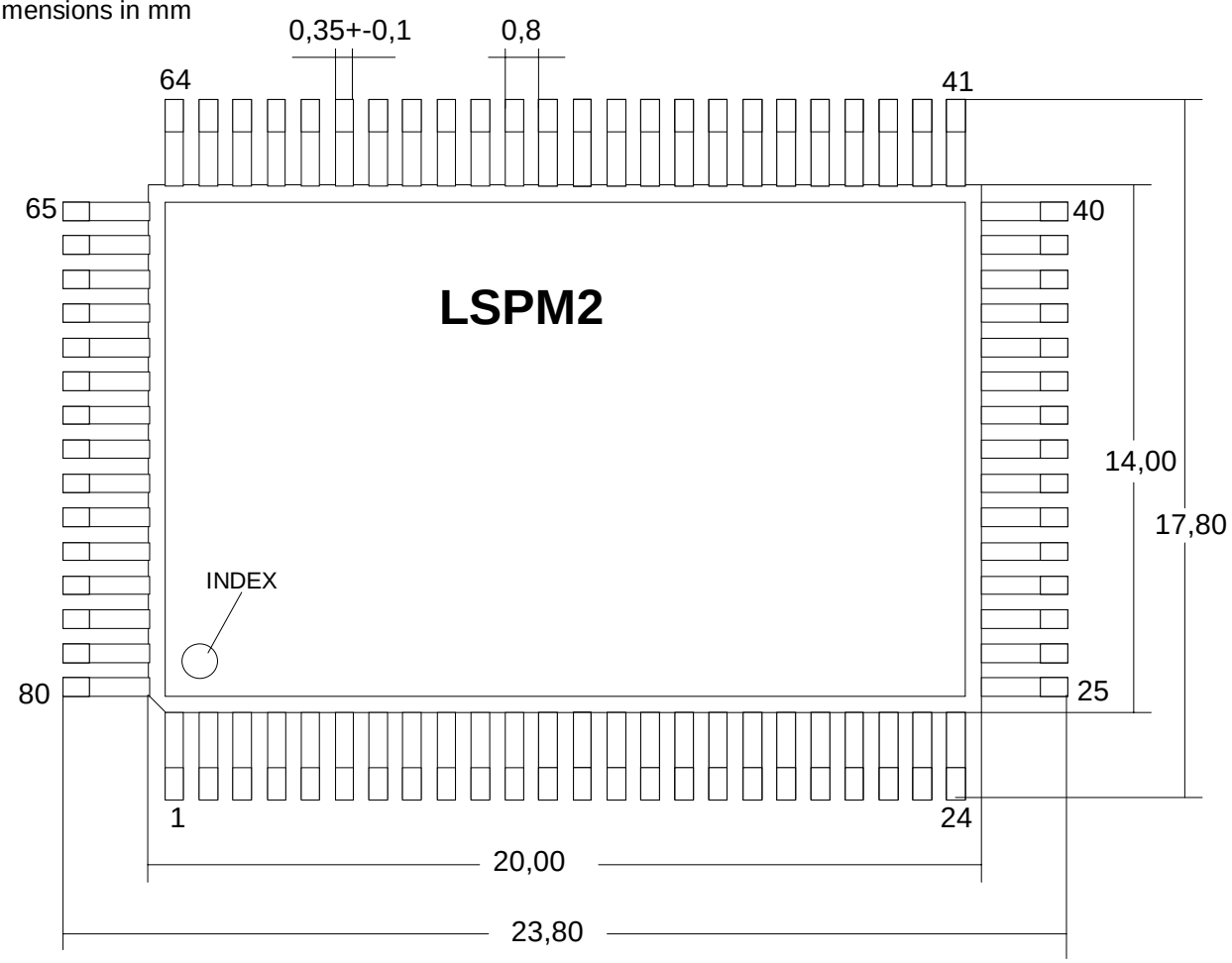
Bidirectional pins:	Qty.	I/O	Type	Buffer
PA7...0	8	I/O	Schmitt trigger	4 mA buffer
PB7...0	8	I/O	Schmitt trigger	4 mA buffer
PC7...0	8	I/O	Schmitt trigger	4 mA buffer
PD7...0	8	I/O	Schmitt trigger	4 mA buffer

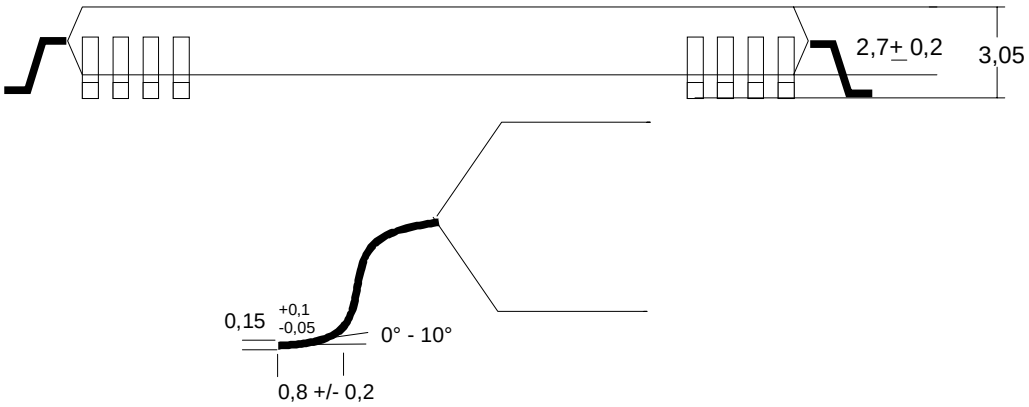
Power supply 7 VDD / 9 VSS

Total 80 Pins

Housing

All dimensions in mm





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Information on handling:

The ESD safety measures must always be observed on all electronic components.

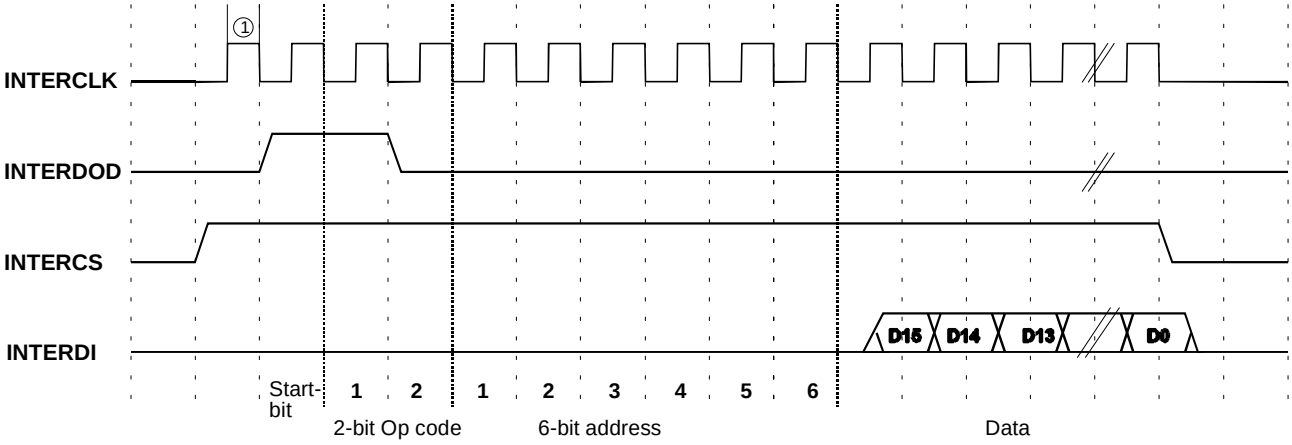
The LSPM2-ASIC is a component subject to the risk of cracking and must be handled accordingly.

The LSPM2 must be dried before processing. The component must be dried for 24 hours at 125^{O}C and then processed within a period of 48 hours. This drying process may be carried out only once owing to component solderability. Also ensure that the pins of the LSPM2 are not bent. Proper processing can be guaranteed only if the deviation from flatness is less than 0.1 mm. The LSPM2-ASIC is approved for infrared soldering with soldering profile in accordance with CECC00802.

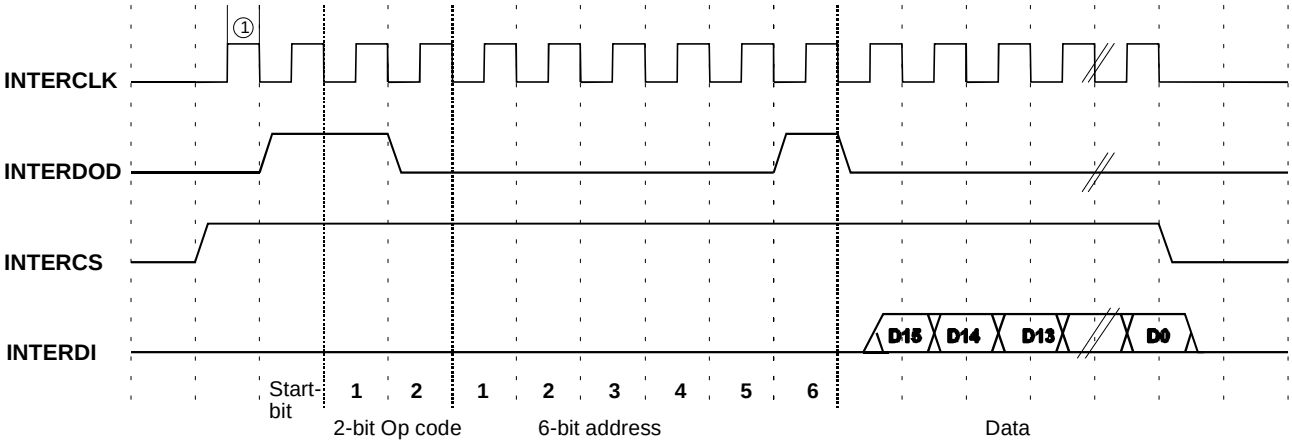
7 Timings

7.1 EEPROM

EEPROM READ cycle Op code 10 (example address 000 000b)

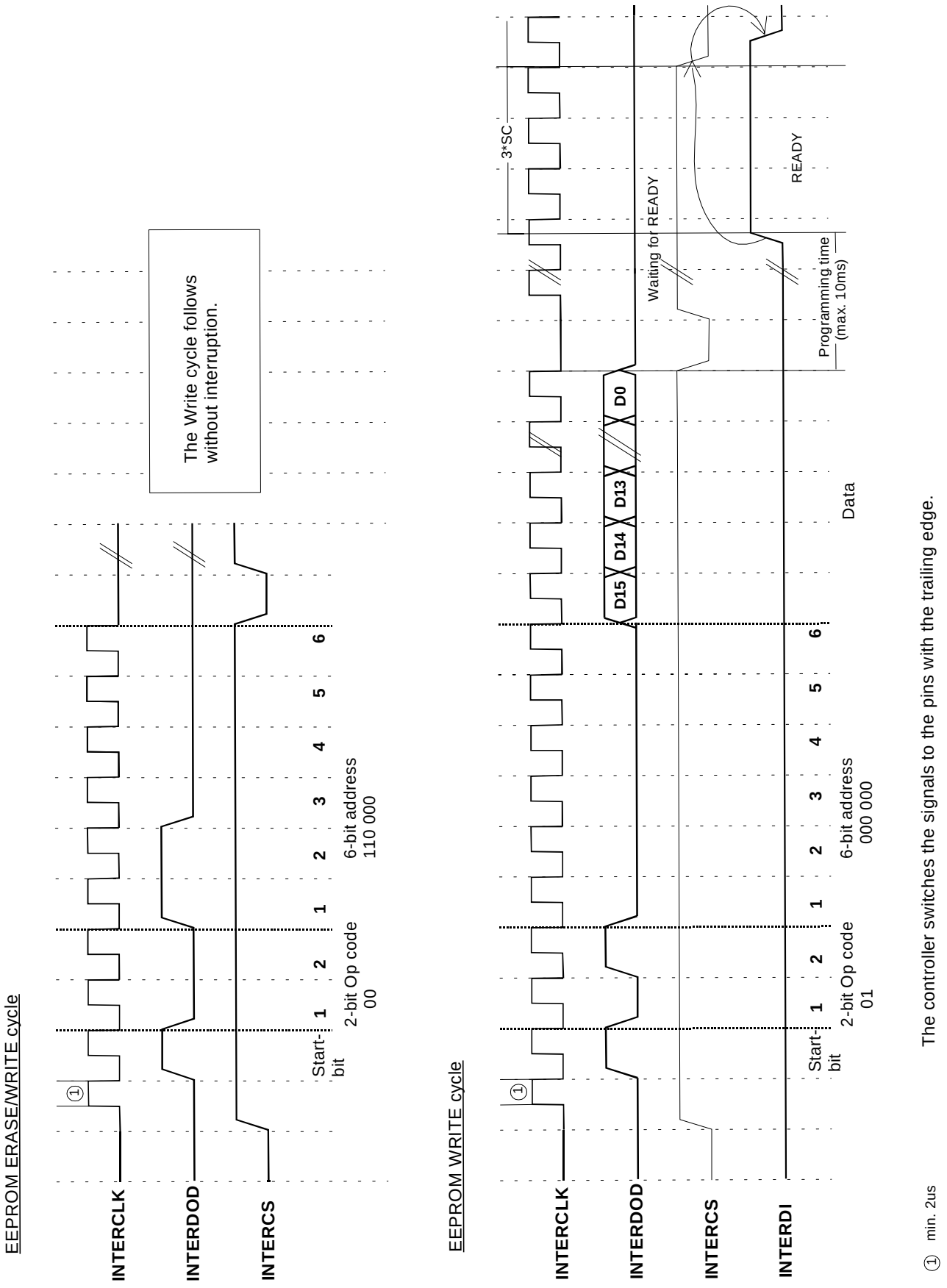


EEPROM READ cycle Op code 10 (example address 000 001b)



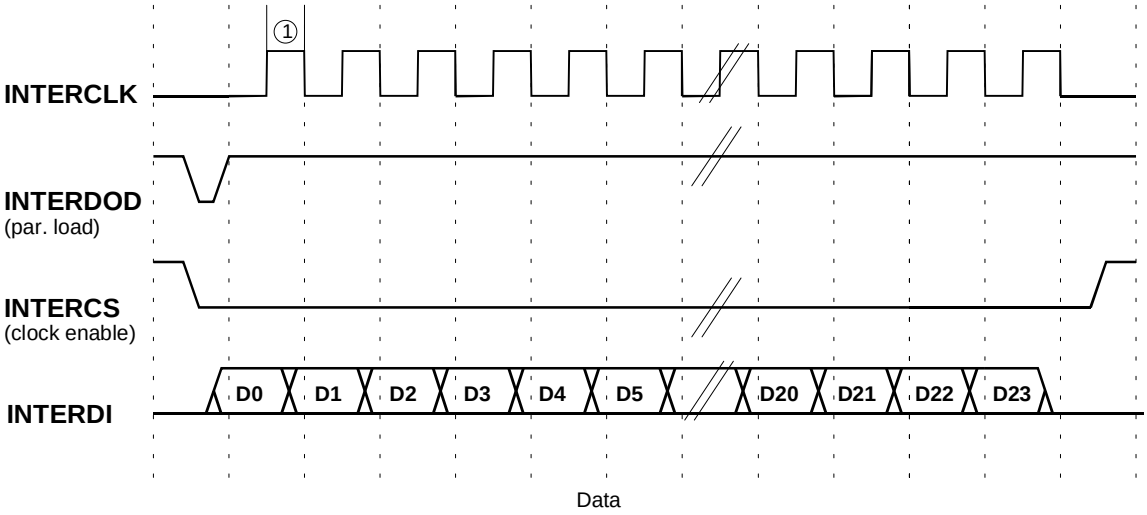
① min. 2µs The controller switches the signals to the pins with the trailing edge.

EEPROM ERASE/WRITE-Zyklus



7.2 Shift register

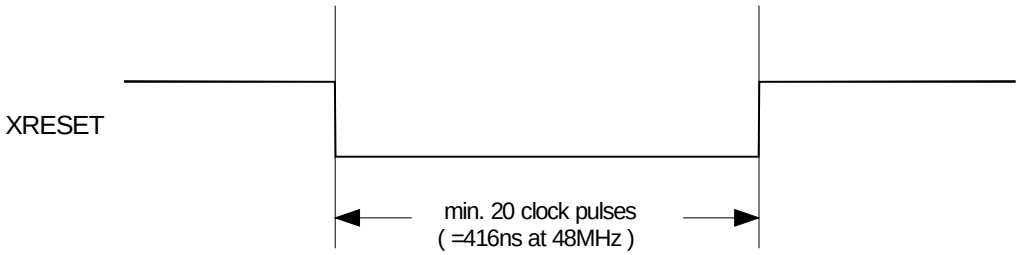
Shift register READ cycle



Data bit : D0 - D7 TS address
D8 - D23 PNO ID number

① min. 2us The controller switches the signals to the pins with the trailing edge.

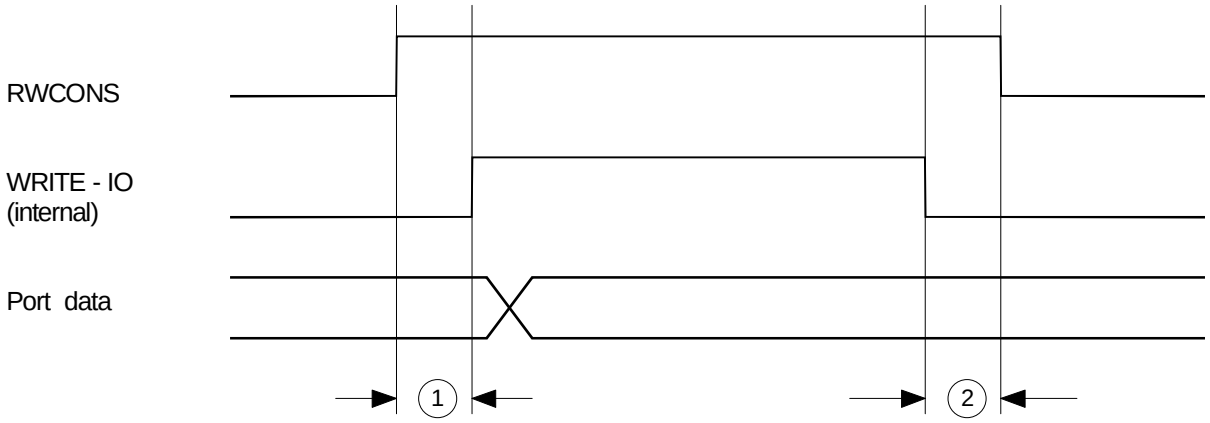
7.3 RESET



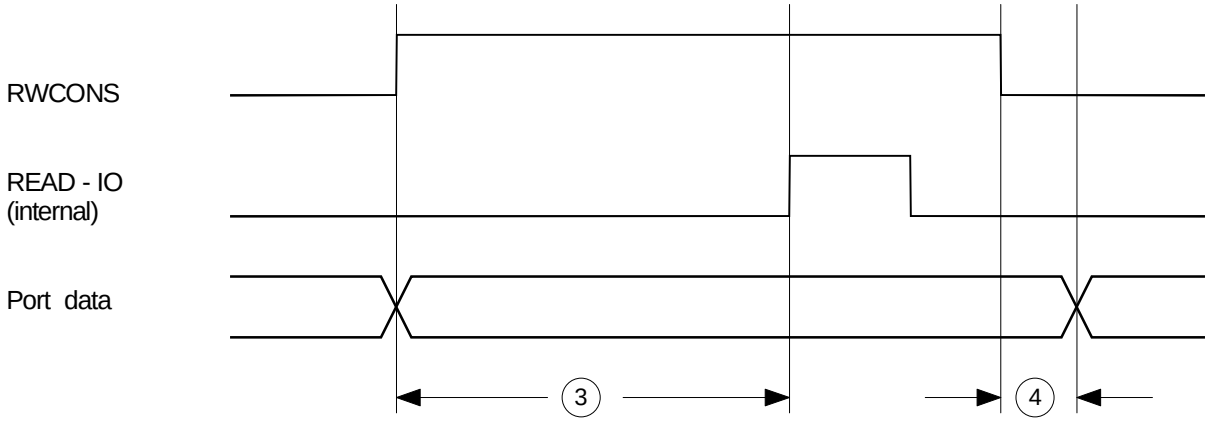
A spike filter is integrated upstream of the reset logic. This filter filters noise spikes up to a length of one clock pulse in order to prevent interference on the RESET line.

7.4 Consistency signal RWCONS

Write timing: The user can switch external latches transparently for instance with RWCONS in order to accept new data from the ports programmed to Output.



Read timing: The user can freeze external latches for instance with RWCONS in order to accept consistent data at the ports programmed to Input ("Snapshot" option).



No.	Symbol	Parameter		Unit
1	$RWCONS_{SETUP}$	RWCONS activ to Write from MS	1	TBit*
2	$RWCONS_{HOLD}$	RWCONS inactiv to Write from MS	1	TBit*
3	D_{SETUP}	Data - Setup after RWCONS active	1	TBit*
4	D_{HOLD}	Data - Hold after RWCONS inactiv	0	ns

*: 1 TBit =104µs at 9,6kBd , 1 TBit = 83ns at 12MBd

8 Address Directory

Profibus User Organization

PNO
Business Office
Mr. Volz
Haid- und Neu- Straße 7
76131 Karlsruhe
Tel.: (0721) 9658-590

Technical reference partners in the interface center

Siemens AG
AUT 7 B1 T2
Mr. Frieß and Mr. Schmidt

Mailing address:
Post Office Box 2355
90713 Fürth

Internal address:
Würzburgerstr.121
90766 Fürth

Tel.: (0911) 750 - 2072
2079
Fax (0911) 750 - 2100

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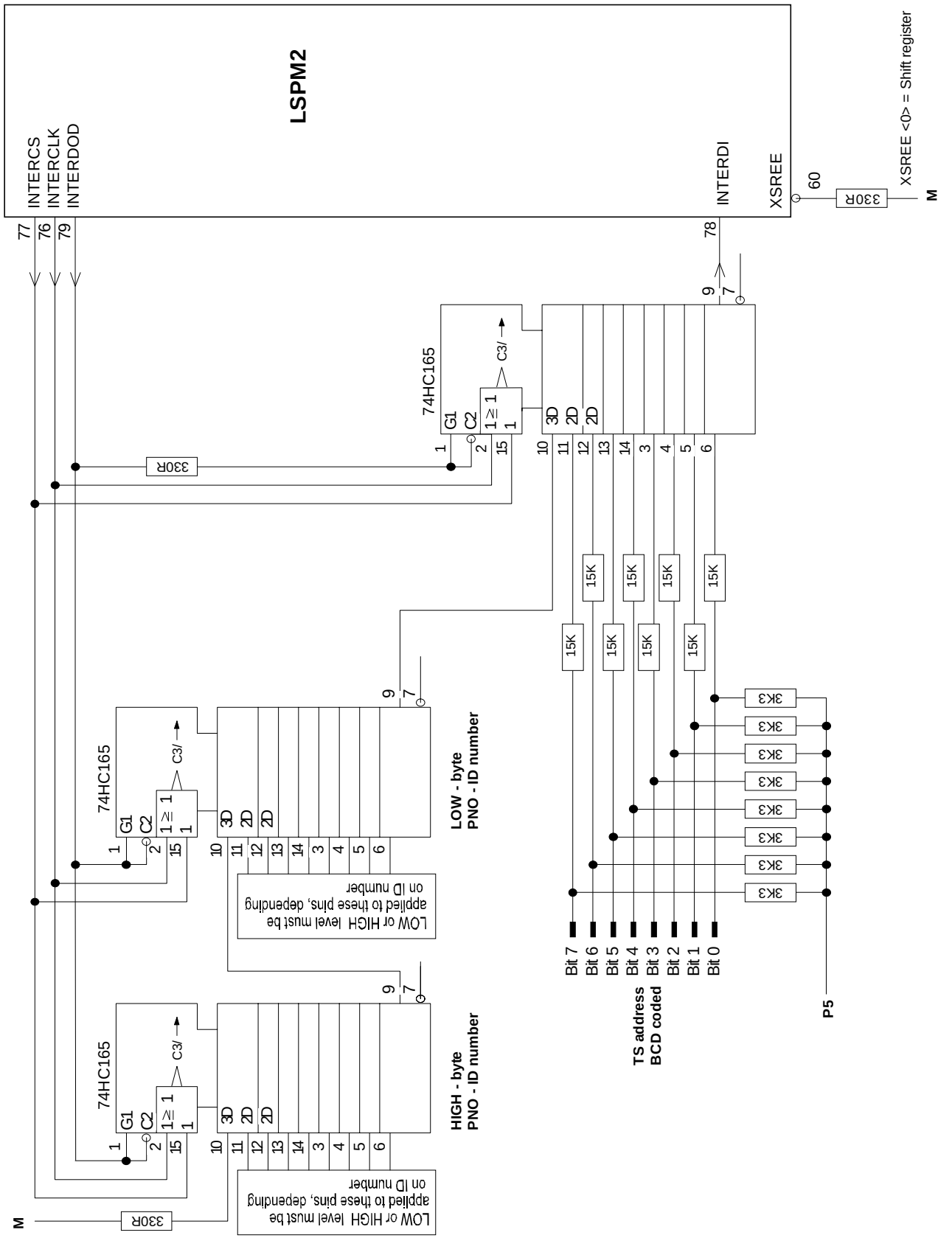
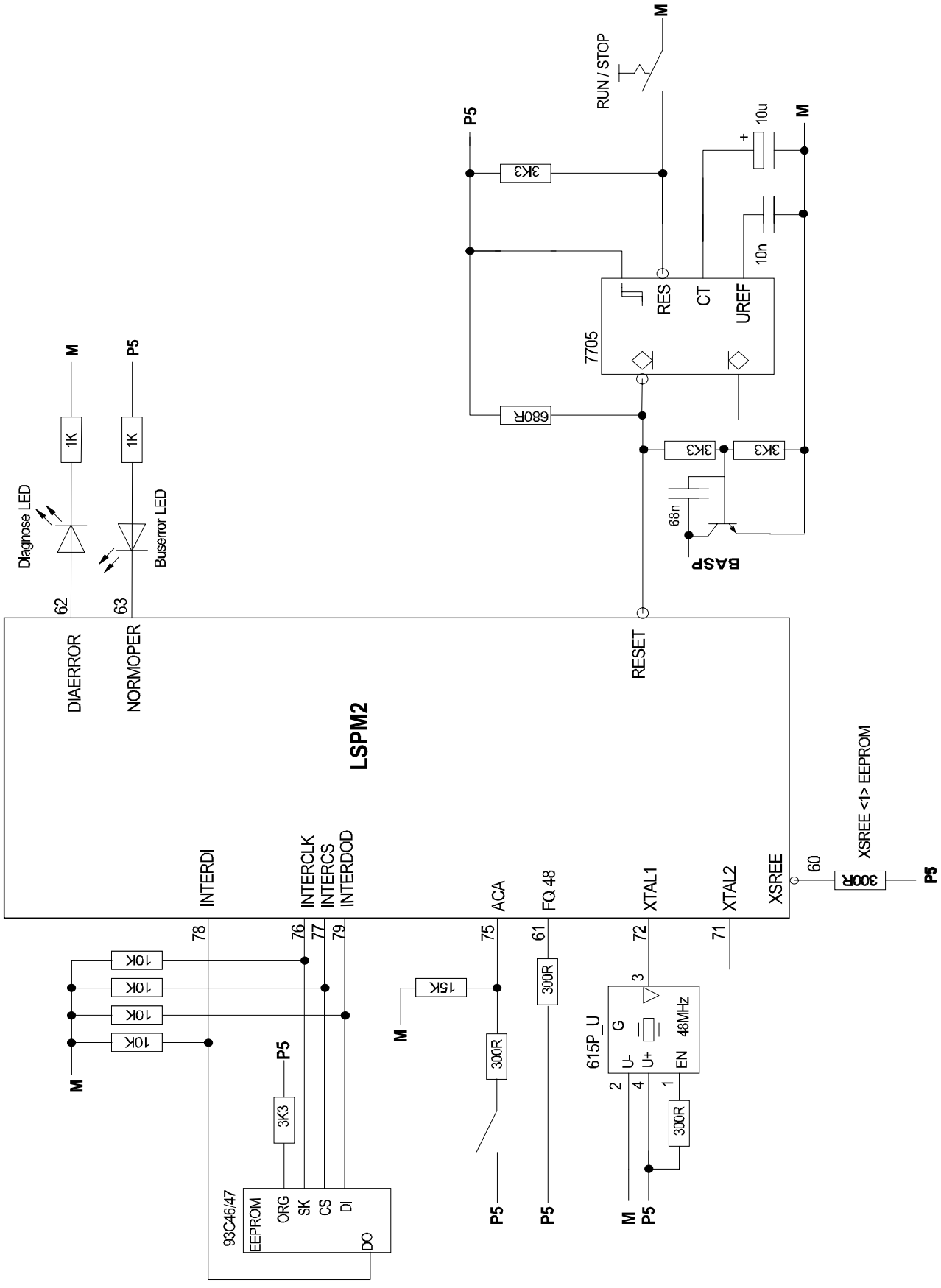
Tel.: 0911 - 737972

9 Circuit examples

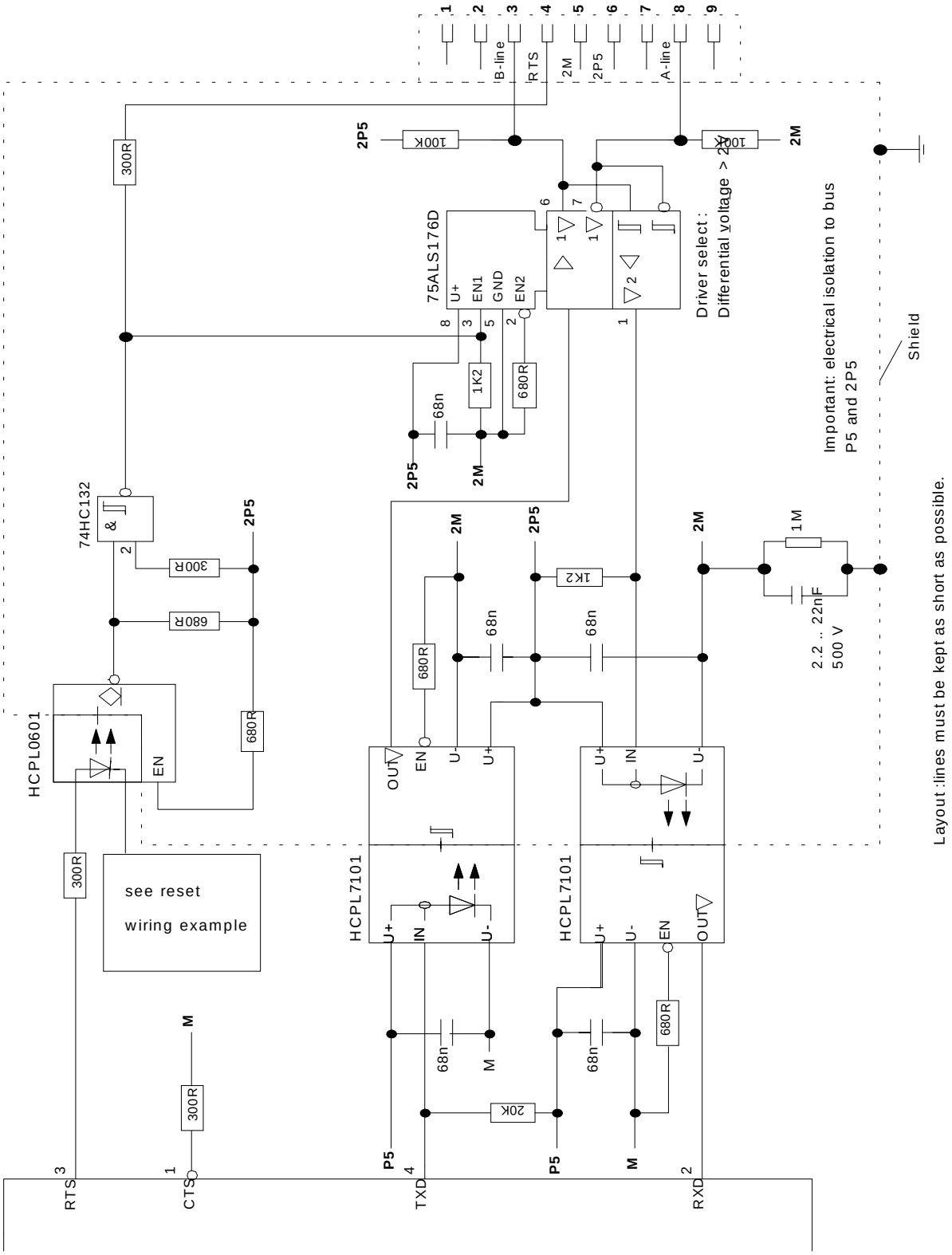
9.1 Shift register



9.2 Wiring example - EEPROM , ext. oscillator , error indicator and RESET



9.3 Wiring Example - PROFIBUS Interface

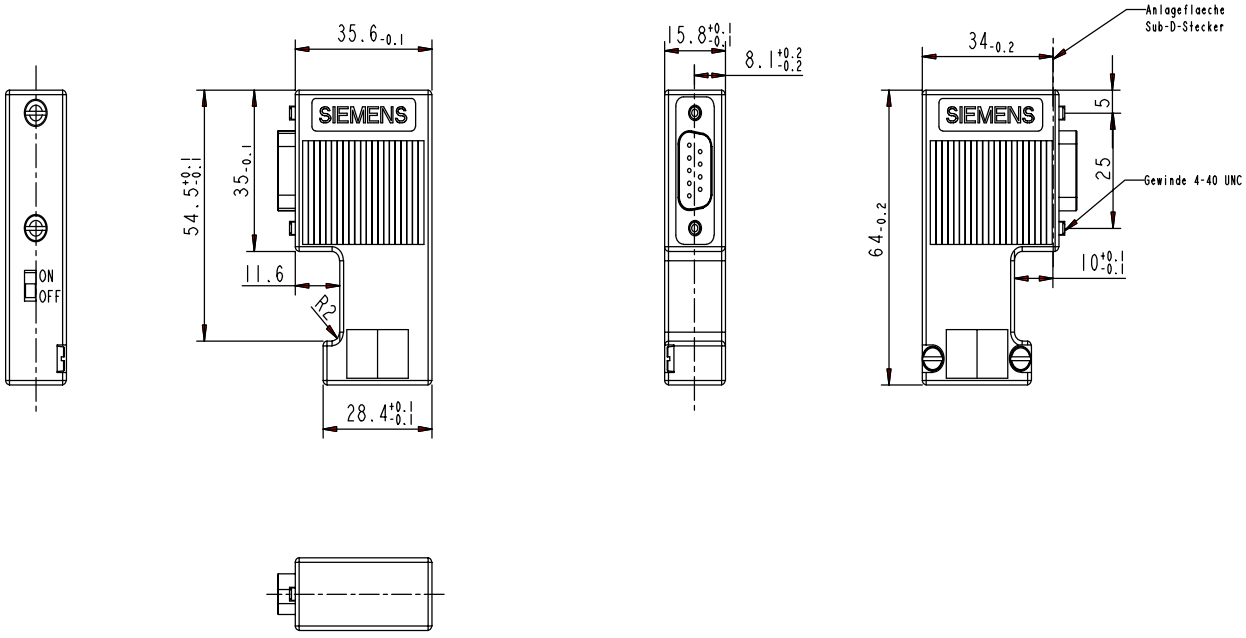


10 Bus Connection

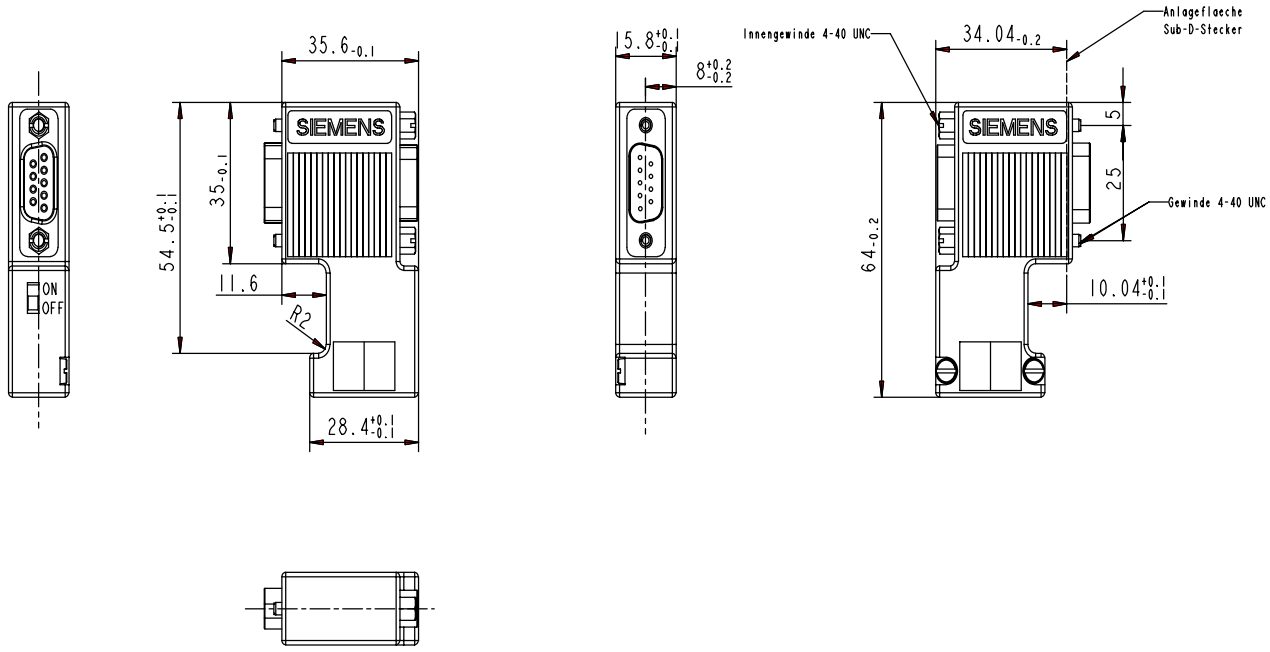
The bus can be connected using the following standard connectors, amongst others, in accordance with PROFIBUS-DP Standard:

MLFB-No.	Notes	Colour of the connector housing
6ES7 972 - 0BA00 - 0XA0	without PG gland	anthracite
6ES7 972 - 0BB00 - 0XA0	with PG gland	anthracite

Dimension drawings:



L2 bus connector: 6ES7 972 0BA00- 0XA0



L2 bus connector: 6ES7 972 - 0BB00 - 0XA0

The slide switch on the rear side of the bus connector must be set to position “ON” in order to connect the bus terminating resistor.

Lines A and B of the incoming and outgoing bus cable must each be connected via separate screw-type terminals.

Siemens AG
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