SIMATIC NET

SPC41 Siemens PROFIBUS Controller

User Description Date: October 1998

SIEMENS

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(Siemens PROFIBUS Controller)

Version: V1.1

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Liability Exclusion
We have tested the contents of this document regarding agreement with the hardware and software described. Nevertheless, there may be deviations, and we don't guarantee complete agreement. The data in the document is tested periodically, however. Required corrections are included in subsequent versions. We gratefully accept suggestions for improvement

Subject to technical changes.

Inhaltsverzeichnis

1 Introduction

The ASIC SPC41 is the successor to the slave ASIC SPC4. In this first version of the documentation, the differences with respect to the existing SPC4 are described; that is, the existing SPC4 documentation is to be taken note of.

In comparison to the SPC4, the SPC41 provides expansions that are enabled via software switches, so that the SPC41 can be operated functionally compatible with the SPC4:

- The RAM has been enlarged from 1.5 kByte to 2 kByte
- The fail-safe mode has been integrated
- Clock time synchronization is also permitted for DP
- Integration of the interface for pulse duration modulation as counterpart to SIM1
- Manchester receiver: quick synchronization has been improved, and the integration window has been widened from 10 microseconds to 14 microseconds
- Synchronization with preamble 1 byte is now possible
- Modus Motorola asynchronous without external FF is now possible

2 Function Expansions in the SPC41

2.1 RAM Expansion

The internal RAM of the SPC41 has been expanded from 1.5 kByte to 2kByte, in order to be able to handle more productive data. The internal address area now ranges from 000H to 7FFH. The access mechanism via an address window the size of 1 kByte continues to exist as usual; that is, the additional 256 bytes are accessible by programming the base pointer correspondingly.

2.2 Additional Parameters of the SPC41

The Mode Register 2 of the SPC4 has been expanded by three bits for the SPC41:

Mode Register 2 (can only be written to)

Address	Bit Position								Designation
Control Register	7	6	5	4	3	2	1	0	
31AH	EN-DDB-MODE	EN-CLOCK-SYNC	SPEC-CLEAR MODE	CHECK-GCT-RESBITS-OFF	CHECK-GCT-LENGTH-OFF	X86	XINTCI	XHOLD TOKEN	Mode-Reg2 7..0

Bit 0-4 Refer to SPC4
Bit 5 SPEC-CLEAR MODE
In the Spec_Clear_Mode (fail-safe mode), the SPC41 accepts, in the Clear Mode of the PROFIBUS master, data messages with the net data length 0.
0 = Fail Safe Mode turned off
1 = Fail Safe Mode turned on
Bit 6 EN-CLOCK-SYNC (clock time synchronization)
XPB/PA = 0 (Profibus Mode):
0 = No clocktime synchronization (state after reset); that is, SM2 Time0/1 messages are filtered
1 = Clocktime synchronization for several clocktime masters switched on
XPB/PA = 1 (PA Mode):
0 = Clocktime synchronization for the SPC4 is set.
1 = Clocktime synchronization for several clocktime masters is switched on
Bit 7 EN-DDB-MODE
XPB/PA = 0 (Profibus Mode):
0 = All DDB messages are filtered (state after reset)
1 = DDB procedure is enabled
XPB/PA = 1 (PA Mode):
0 = : DDB procedure is always enabled.
1 = : DDB procedure is always enabled.

The expansion of Mode Register 2 in the SPC41 is compatible with the SPC4 regarding software, since the current server software respectively assigns 0 to Bits 5 to 7 of the data bus when parameters are assigned to the register.

Mode Register 3 has been added to the SPC41:

Mode Register 3 (can only be written to)

Address Control Register	Bit Position								Designation
	7	6	5	4	3	2	1	0	
31BH						Quick_Sync_New	Debug	Pulse Modulation	Mode Reg37..0

Bit 0 Pulse Modulation

Pulse Modulation for SIM1

0 = Pulse modulation is switched off (state after reset).

1 = Pulse modulation is enabled.

Bit 1 Debug

The SPC41 triggers an interrupt as soon as a micro-sequencer command is executed that was specified previously.

0 = Debug interrupt is switched off (state after reset)

1 = reserved

Bit 2 Quick_Sync_New

Quick synchronizer in the Manchester receiver

0 = Improvement is inactive (state after reset)

1 = Improvement is active

2.3 Fail-Safe Mode

An additional Mode Register bit “Spec Clear Mode” (Bit 5 in Mode Register 2) enables the fail-safe mode.

The bits “IND-N CLEARED” and “IND-U Cleared” are added to the access byte of the default SAP:

Access Byte(3..0) := Access-Value
Access Byte(4) := RUP-N Valid
Access Byte(5) := IND-N Valid
Access Byte(6) := IND-N Cleared
Access Byte(7) := IND-U Cleared

Bit Position								Designation
7	6	5	4	3	2	1	0	
IND-U Cleared	IND-N Cleared	IND-N	RUP-N	Access Value				Access Byte

Bit 0-3 Access Value
Bit 4 RUP-N Valid (only in the case of DEFAULT SAP)
Bit 5 IND-N Valid (only in the case of DEFAULT SAP)
Bit 6 IND-U Cleared

The user has to set the Bit ”IND-U Cleared” when the fail-safe mode is entered, and to reset it when the fail safe mode is exited. The SPC41 does not modify this bit. However, the SPC41 does poll it if ”Spec-Clear-Mode=1”, and a message ”Read Output Data” is received in the DP mode.

0 = if the application is not in the fail-safe mode; that is, the application uses the data of the Indication Buffer U as output data. If ”Spec-Clear-Mode = 1”, the user has to reset ”IND-U Cleared=0” if he wants to update his output data, and ”IND-N Valid=1” and ”IND-N Cleared=0”.

1 = if the application is in the fail-safe mode; that is, the application uses the Clear coding as output data. The data in the Indication Buffer U is then invalid. If ”Spec-Clear-Mode = 1”, the user has to set ”IND-U Cleared=1” if he wants to update his output data, and ”IND-N Valid=1” and ”IND-N Cleared=1”.

Bit 7 IND-N Cleared

The bit ”IND-N Cleared” is to be evaluated only if ”IND-N Valid = 1”.
If ”IND-N Valid = 1”, the following applies:

0 = if the output data in Indication Buffer N can be accepted

1 = if the output data in Indication Buffer N is to be replaced through the corresponding Clear coding. In Indication Buffer N, the output data that was received last is entered.

With the parameter assignment “Spec-Clear Mode = 1”, the SPC41 also accepts data messages without output data if the control unit is in the state “Data Exchange”. This applies regardless of the value of the parameterized indication buffer length in the default SAP of the SPC41. If “Spec-Clear Mode = 1”, the SPC41 executes the following actions after receiving such a message with the net data length = 0 (if parameterized indication buffer length > 0):

- generate interrupt “Watchdog Reset”
- generate interrupt “Output Data Exchange”
- respond with input data
- set IND-N Valid := 1 and IND-N Cleared := 1

If the user updates his output data by exchanging the Indication Buffers N and U, he recognizes by “IND-N Valid = 1” and “IND-N Cleared = 1” that the output data is to be replaced through the corresponding Clear coding. Also, the data -received as subscriber- of DDB response messages in the indication queue is to be replaced through the corresponding Clear coding. The output data is not cleared by the SPC41 in the Clear state; that is, it is not overwritten with 00H.

If the SPC41 receives a message “read output data”, it checks the bit “IND-U Cleared”. If “IND-U Cleared =1”, the SPC41 responds with 00H as output data.

With the parameterization “Spec-Clear Mode = 1”, the SPC41 does not clear the output data even if it executes Leave Master, or receives a global control message with “Clear Data = 1”. To identify the Clear state, the SPC41 sets “IND-N Valid = 1” and “IND-N Cleared = 1”.

If “Spec_Clear_Mode = 0”, the SPC41 behaves like the SPC4. Fail-safe messages are not recognized ; in the Clear mode, output data is overwritten with 00H. IND-N Cleared is not set. IND_U Cleared is don’t care.

Attention:
The execution time tCLR that the SPC41 needs for clearing the output data depends on the indication buffer length n, and the baudrate. The following applies approximately to 12 MBaud: (15 + n) bit pulses = tCLR = (20 + 1.5n) bit pulses. The following applies approximately to baudrates less than 3 MBaud: tCLR = (20 + 0.5n) bit pulses. Thus, the SPC41 needs, at 31.25 kBaud, approximately 150 bit pulses for clearing 256 bytes. Since the bus parameter TID1 (= 37 bit pulses) is considerably shorter in the case of this baudrate, request messages to the SPC41 may be lost.

2.4 Clocktime Synchronization

The SPC41 supports two procedures of clocktime synchronization. The requested procedure is selected with the parameter bit “En Clock Sync” (Bit 6 in Mode Register 2).

With “En Clock Sync :=0” (state after reset), the SPC41 behaves like the SPC4 in the case of clocktime synchronization. Clocktime synchronization is then available only in the PA mode (XPB/PA = 1). In the Profibus mode (XPB/PA = 0), the SM2-Time0/1 messages are filtered by the SPC41.

With “En Clock Sync := 1”, the SPC41 supports a clocktime synchronization procedure that also permits the operation of several clocktime masters. This procedures is available in the PA mode as well as in the Profibus mode.

The delay timer integrated in the SPC41 is increased to 24 bits (SPC4: 16 bit delay timer). In the case of the SPC41 (as is the case with the SPC4), each overrun of the integrated delay timer generates an interrupt “Del Tim Overrun (= Bit 4 of the interrupt register). This interrupt makes it possible for the user to expand the internal delay timer as required.

Attention:
If the SPC4_1 is configured so that the 24 bit delay timer is used, the SPC4_1 returns the interrupt Delay Timer Overrun only if the value of the Factor Delay Timer Clock Register is 0.

In order to be compatible with the SPC4, the delay timer of the SPC41 is limited to 16 bits in the PA mode (XPB/PA = 1); that is, the interrupt “Del Tim Overrun” is generated if the 16 bit timer overflows.

In the Profibus mode (XPB/PA = 0), the delay timer has a width of 24 bits. The interrupt “Del Tim Overrun” is generated if the 24 bit timer overflows. Bits 23 to 16 of the delay timer can be read out under the address 310H.

2.5 DDB Procedure

With “En DDB Mode := 1”, (Bit 7 in Mode Register 2), the DDB procedure is enabled in the Profibus mode (XPB/PA = 1) of the SPC41. If this bit is not set, all DDB messages are filtered.

The DDB procedure is always enabled in the PA mode (XPB/PA = 1) of the SPC41. The parameter byte “En DDB Mode” is don’t care in the PA mode.

In the case of the SPC4 and the SPC41, the DDB procedure is limited to the default SAP. All other SAPs can’t be operated with DDB. The default SAP is the only SAP that makes separate resources for the SDN/DDB station table and for the response data (reply update buffers D, N, U) available in the DP mode. If the DP mode = 0, either the station table for filtering SDN- or DDB response messages, or a reply-on-indication buffer for response data is available to the default SAP (as to the other SAPs).

2.6 Additional Interrupt of the SPC41

The interrupt register of the SPC4 is expanded with Bit 12 in the case of the SPC41:

Address Control Register	Bit Position								Designation
	15	14	13	12	11	10	9	8	
303H (Intel)	IND	IND-PRE	FIFO Overflow	Ignore_ Delay Timer Overrun	Leave Master	Write Violation	Timeout	Mem Overflow	Int--Reg 7 15..8

Bit1-11	Refer to SPC4
Bit 12	Ignore_Delay Timer Overrun In the state W-T1 of the SM2 Time Slave Control Unit, an SM2 Time0 message was received from the current clocktime master. In the PA mode, this interrupt is always masked.
13-15	Refer to SPC4

2.7 Pulse Modulation in the SPC41

In the SPC41, circuit components are integrated for a direct connection SIM1-Optocoupler-SPC41 (Profibus PA connection), under utilizaton of the power-saving interface of the SIM1. A separate interface circuit is no longer needed.

The circuit is laid out for one single application case only:

Profibus-PA
Operating Frequency at the SPC41: 2 MHz
Baudrate: 31.25 kBaud

The messages received by the SIM1 are not transmitted to the SPC41 in their original form. To save power, the SIM1 converts the message into a series of short pulses. It therefore appears at the SPC41 in the following form:
Each rising edge in the message results in a high pulse with a width of 5µs, each falling edge in a high pulse with a width of 2µs. Between the pulses, the signal has the level 0.

When the SPC41 transmits a message, this pulse sequence is generated from the message to be sent. The only difference is the inverted polarity: To trigger the opto-couplers, low pulses instead of high pulses have to be generated.

Activation:
In order to switch on the pulse modulation, the user has to set the bit Pulse Modulation in the new Mode Register 3 (address 31 BH).

Pulse Modulation (Bit 0): 0: Pulse modulation is switched off (state after reset).
1: Pulse modulation is enabled

2.8 Debug Interrupt

This procedure is for internal testing purposes only.

2.9 Fast Synchronizer in the Manchester Receiver

The SPC41 has an improved fast synchronizer in the Manchester receiver. To activate it, the user has to set the bit Quick_Sync_New in the new Mode Register 3 (address 31BH):

Quick_Sync_New (Bit 2): 0: Improvement is inactive (state after reset)
1: Improvement is active

Fast synchronization means finding the bit center in the preamble of a Manchester message (Profibus PA). The SPC4 positions this time on the fourth message edge in the preamble. The SPC41 attempts to specify this time more exactly by determining the duration of the last high phase and low phase before the fourth edge. From the average of these two numbers, it calculates a correction value that is taken into account when specifying the bit center. Because of this modification, the SPC41 can handle more systematic distortion (all rising or falling edges are delayed by the same amount) than the SPC4.

3 Error Removal

3.1 Synchronization of the RD Signal or the CS Signal of the SPC4

In the case of the SPC4, the later of the two signals RD or CS had to adhere to a set-up time of 8ns prior to the rising edge of the SPC4 pulse.

This timing requirement does not exist for the SPC41.

3.2 Write Accesses in the Mode “Motorola Asynchronous”

Because of a faulty write access of the SPC4 in the mode “Motorola asynchronous” (stored CS), the AS signal of the SPC4 had to be connected to the CS signal of the processor.

The SPC41 can be operated like the SPC4, but makes the connection of the AS signal to its AS pin possible also.

4 Error Description

4.1 SPC41 problems with the ISCLK-Out signal

Unlike the SPC4, the SPC41 does not generate the output clock ISCLK, while it is in RESET mode. For instance, a processor would not be provided with the clock during the RESET mode, if it is connected to the ISCLK signal.

4.2 Problems in the case of the SPC41 with MemLock

A continuous loop may sporadically occur if the memlock cell is scanned (this is necessary, in order to lock the SPC4 for accesses to certain memory areas).
This problem can be bypassed if, in addition to reading out the memlock cell, the bit MEMLOCK == 1 is polled in the status register.

When replacing the SPC4 with the SPC41, this necessary firmware adpatation has to be taken into consideration.

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